

# **Power performance analysis of a Pipelined 8-bit RISC-V inspired processor**

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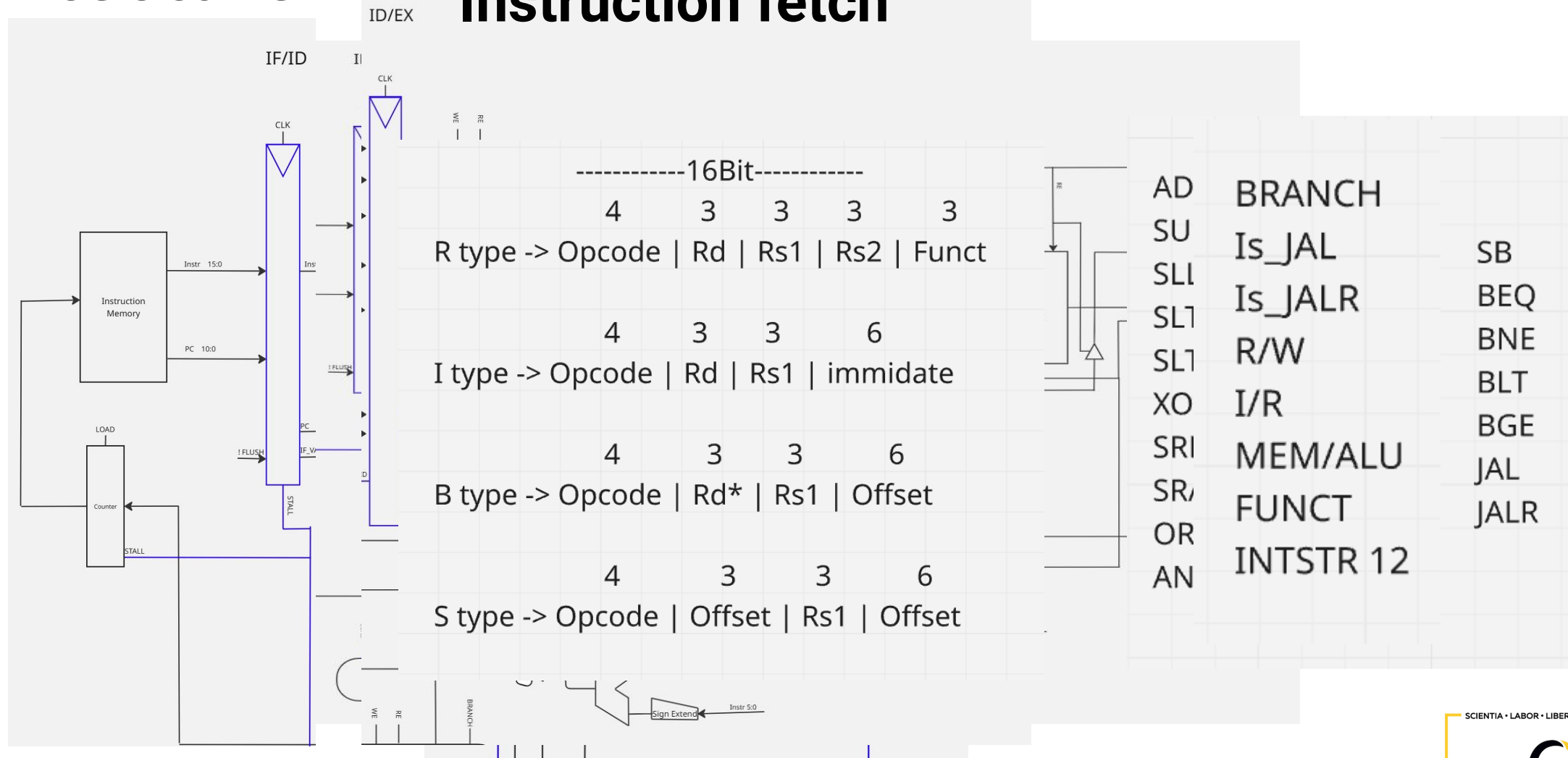
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# Architecture

## Instruction Decode Instruction fetch



# Performance analysis

## Why Pipeline

$$\text{CPI} = 1 + 0.2 \times 0.6 \times 2 + 0.2 \times 1 = 1.44$$

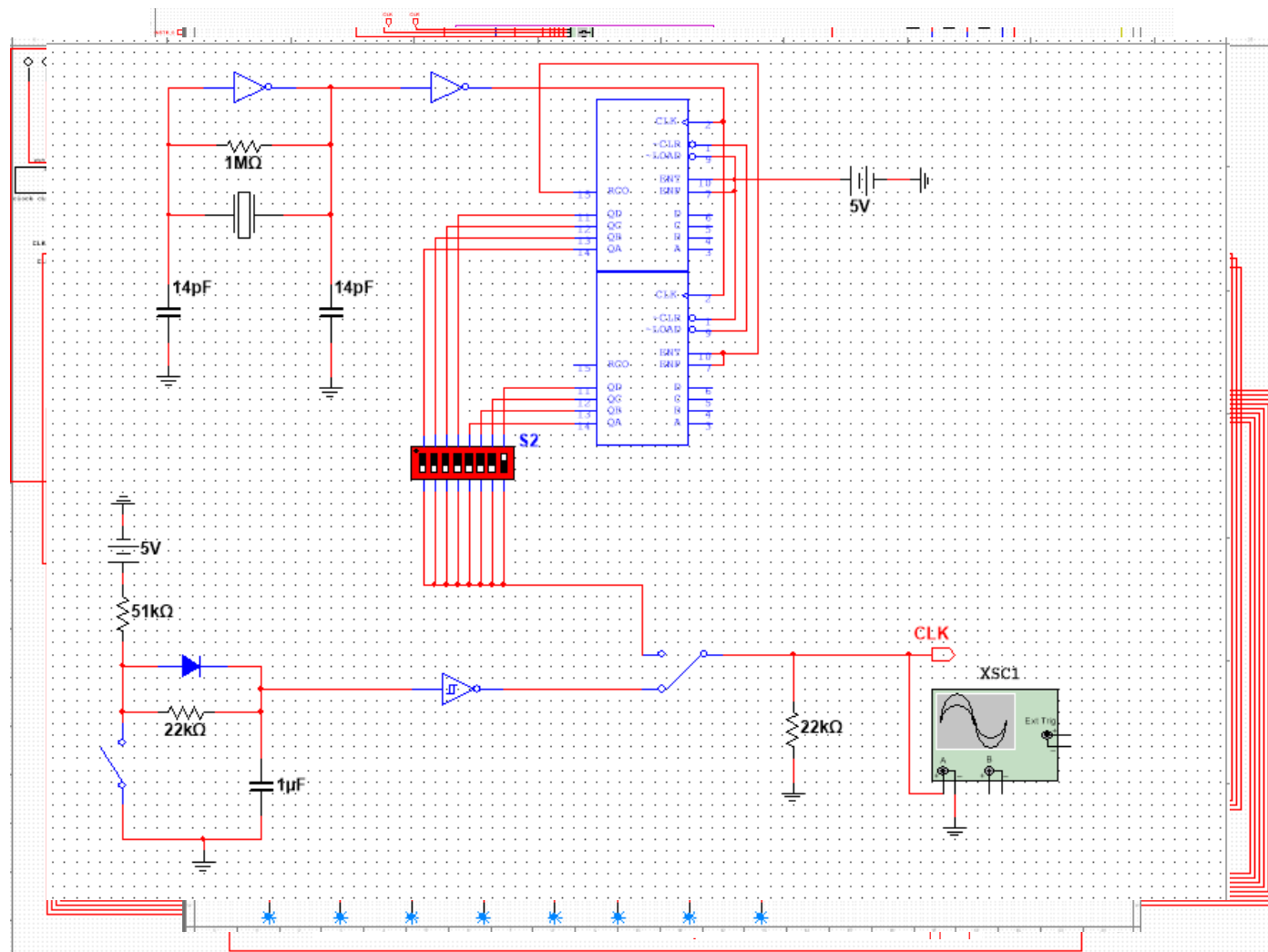
Diagram illustrating the components of the CPI calculation:

- Ideal**: Points to the '1' in the equation.
- Branch instructions**: Points to the '0.2' coefficient.
- Taken branches**: Points to the '0.6' coefficient.
- Instructions lost**: Points to the '2' multiplier.
- RAW Hazard**: Points to the '0.2' coefficient.
- Bubbles**: Points to the '1' multiplier.

$$\text{AVG delay} \rightarrow 1.44 \times 346 = 498\text{ns}$$



# Resistor Simulation

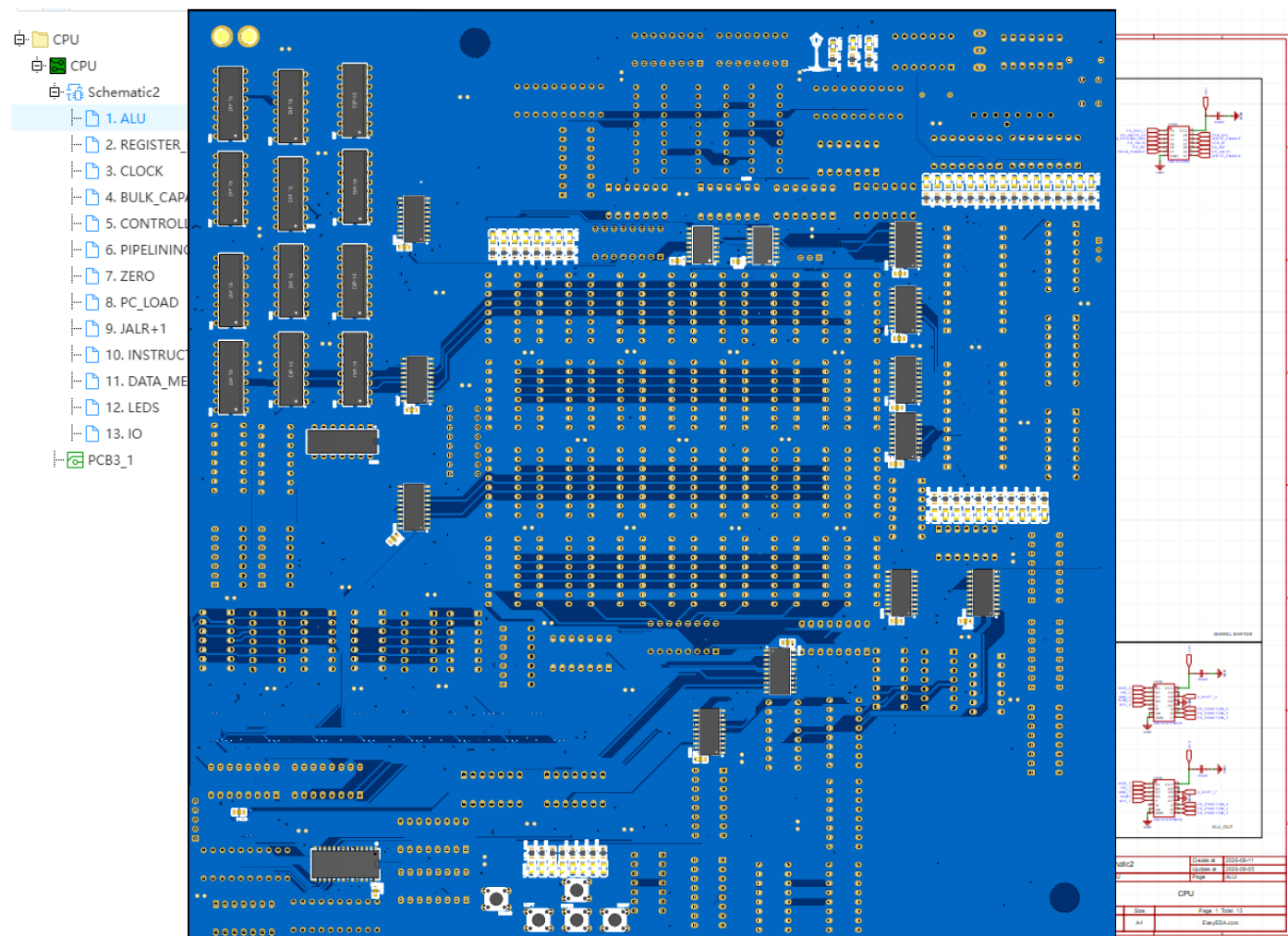


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# PCB



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# Improvements Plan

- **Resolve Branch in Instruction Decode**
- **Make one bit shifter**
- **Add fourth layer in pipeline**
- **Make miniature version of BTB**
- **Do Frequency sweep and measure power/performance**

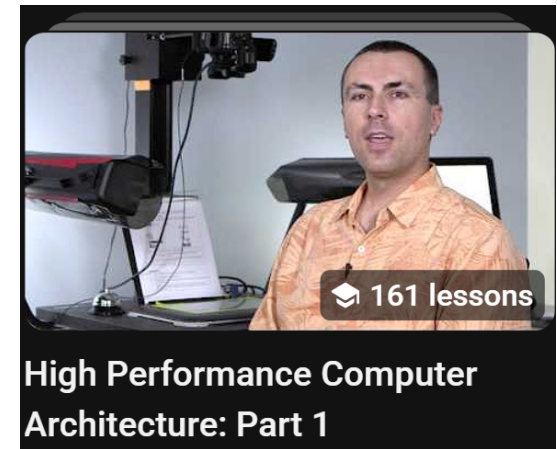
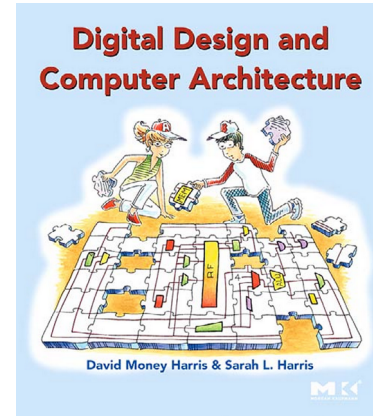
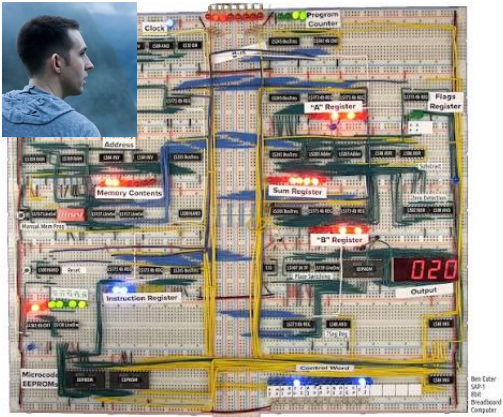


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# Sources



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# Thank you very much



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