

Inter-Microcontroller Low-Cost Phase-Modulated RF Link

A 433 MHz BPSK transmitter from generic discrete parts

Goal, contribution, scope.

What we built

A 433 MHz BPSK transmitter driven by MCU GPIOs: a Qucs-S schematic and an ngspice transient simulation. Low cost switching MOSFETs plus passive components.

What is new here

frequency multiplication, LC filtering. switched-polarity BPSK modulator from generic parts at a \$0.97 bill of materials, with the MCU's PIO doing the timing so the CPU idles.

What the is goal

Move megabits between two microcontrollers using only generic parts.

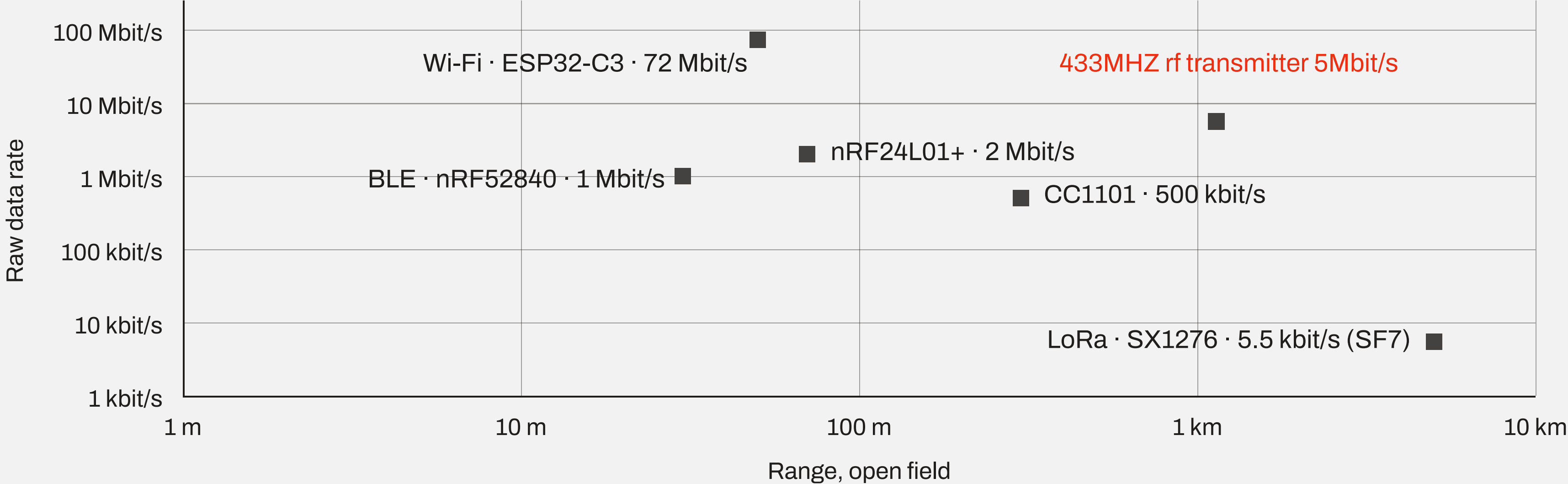
Comparison between Phase and amplitude modulation

OOK: The receiver has to decide "is the carrier on or off" against a threshold. That threshold has to track signal strength, so it drifts with distance, fading and interference.

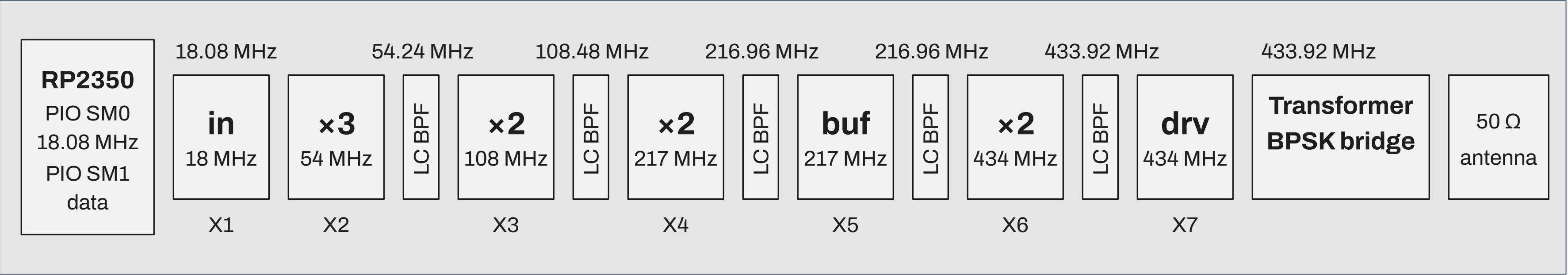
BPSK: phase carries the data. The carrier is always on at full power. The receiver only asks which of two phases it is in, and it compares the signal against itself rather than against a level.

Noise, fading and distance have worse effect on amplitude than phase

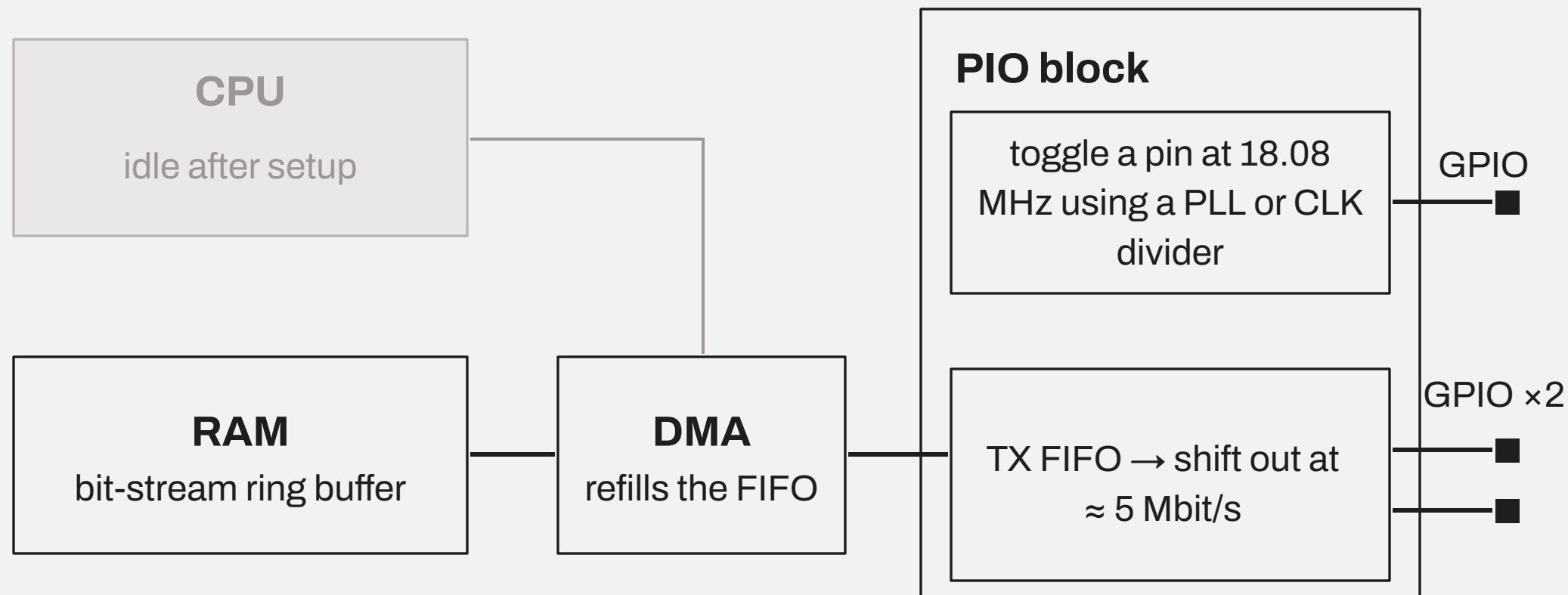
Data rate versus range



System architecture



MCU-side implementation (RP2350)



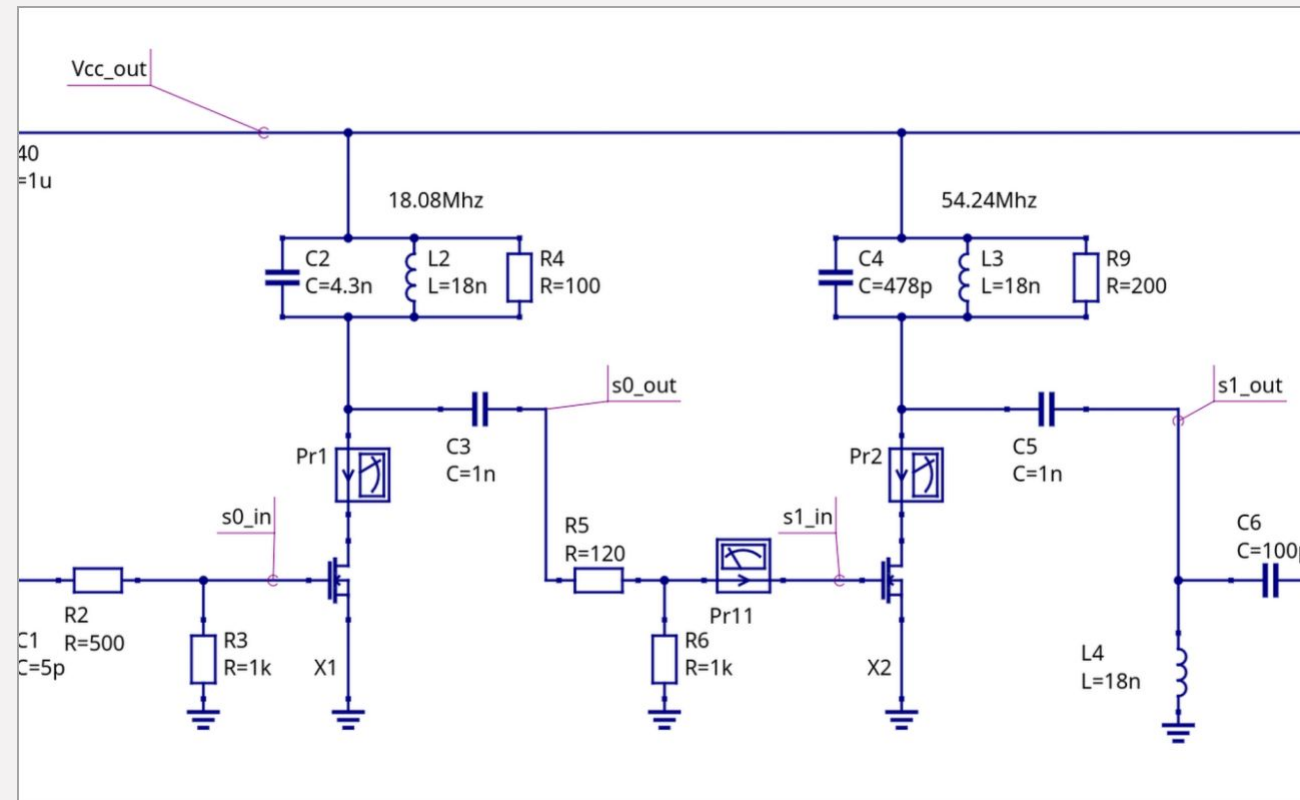
PIO state machines run their own programs from dedicated instruction memory, independent of the cores.

SM0 makes the 18.08 MHz reference, SM1 shifts the bit stream to two complementary GPIOs.

DMA feeds SM1's FIFO from RAM. the CPU sets it up once, then sleeps or runs the application.

Frequency multiplier stage

drain tank at the wanted harmonic



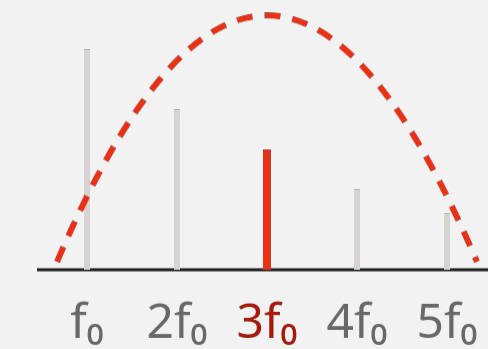
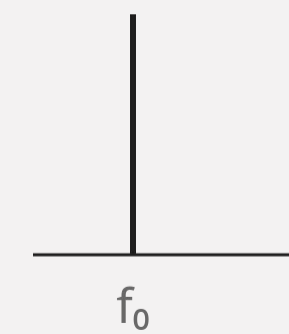
Qucs-S netlist excerpt: input stage, 18.08 MHz -> x3, 54.24 MHz

X2 selects the third harmonic: the gate gives a drain pulse train, the 18 nH / 478 pF tank resonates at 54.3 MHz.

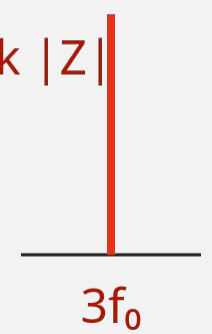
gate: f_0

drain: all harmonics

out: $3f_0$



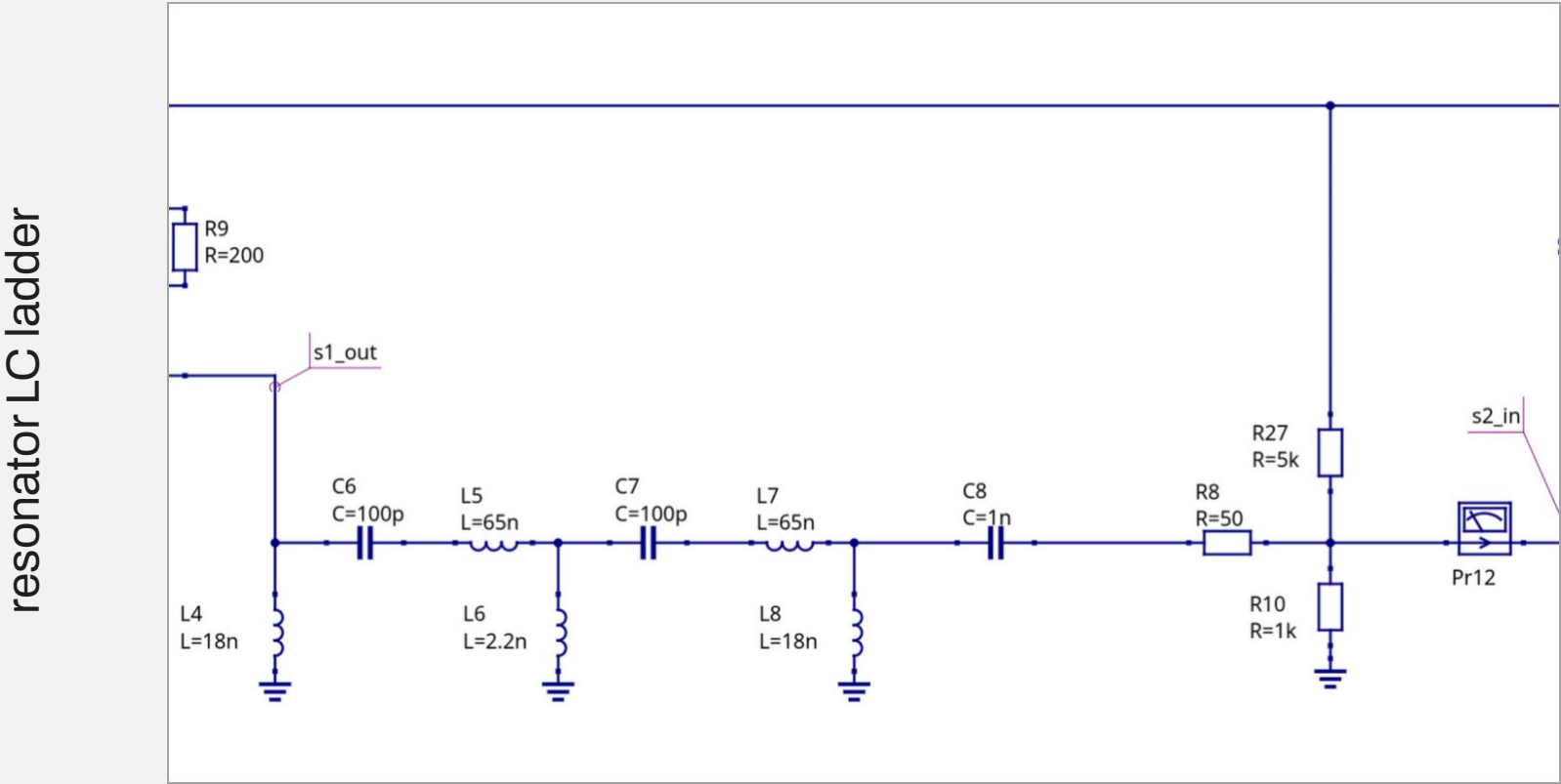
tank $|Z|$



LC tank formula:

$$f_{\text{tank}} = \frac{1}{2\pi\sqrt{L \cdot C}}$$

Interstage filtering



A ladder sits before gate: series L–C resonators with shunt inductors (Chebyshev).

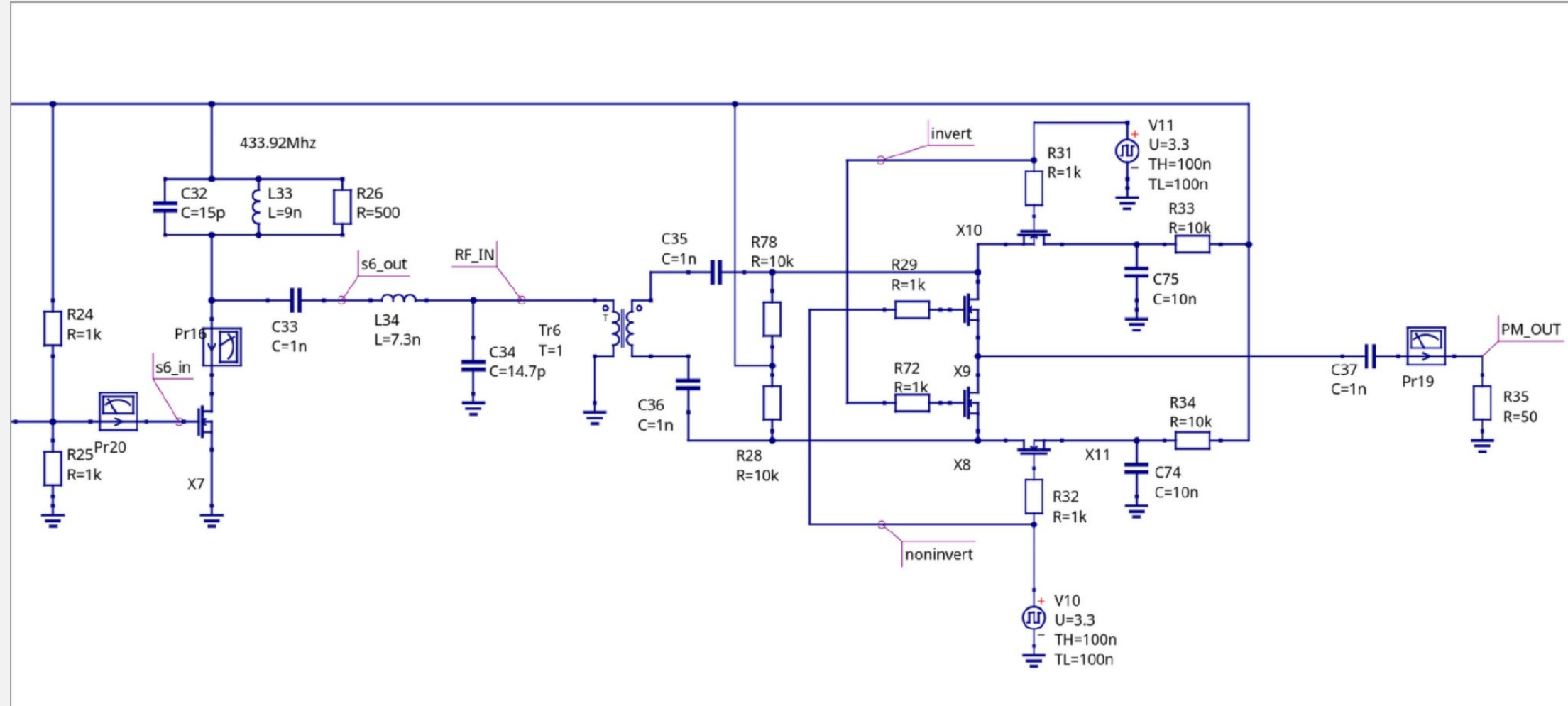
Rejection at each node FFT markers

NODE	WANTED	NEIGHBOUR	LEVEL
X4 drain	217 MHz	108 MHz	–18 dB
after BPF + X5	217 MHz	108 MHz	–89 dB
X6 drain	434 MHz	217 MHz	–2 dB
after BPF + X7	434 MHz	217 MHz	–65 dB

Interstage: Chebyshev.
Output: Bessel

driver, transformer and bridge

Qucs-S schematic

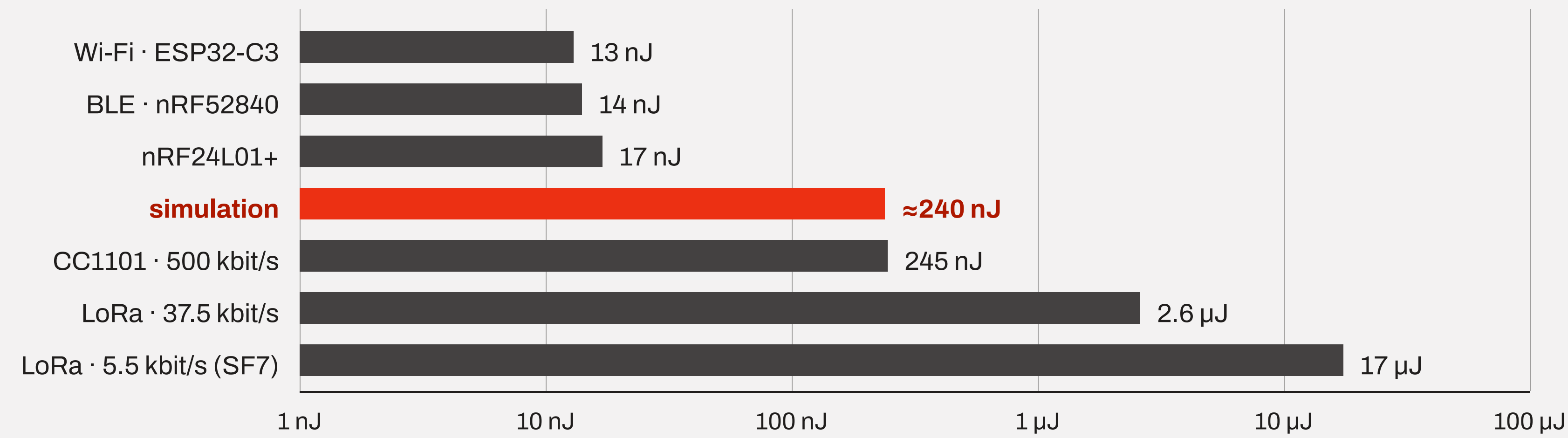


Final stage X7 (433.92 MHz tank) -> L34 / C34 match -> Tr6 (1:1) -> bridge X8–X11 -> C37 -> 50 Ω (PM_OUT)

Results and comparison

RADIO	BAND	RAW DATA RATE	TX POWER	TX-SIDE DC	ENERGY / BIT
BLE · nRF52840	2.4 GHz	1 Mbit/s	0 dBm	14 mW	≈14 nJ
Wi-Fi · ESP32-C3	2.4 GHz	72 Mbit/s	+18.5 dBm	0.91 W	≈13 nJ
nRF24L01+	2.4 GHz	2 Mbit/s	0 dBm	34 mW	≈17 nJ
CC1101	433 MHz	500 kbit/s	+12 dBm	≈120 mW	≈240 nJ
LoRa · SX1276	433/868 MHz	37.5 kbit/s	+13 dBm	96 mW	≈2.6 μJ
simulation	433.9 MHz	≈5 Mbit/s	≈+7.5 dBm	≈1.2 W	≈240 nJ

Energy per bit



Energy per bit = TX-side DC power ÷ raw rate. Beats LoRa by 10–70×, matches the CC1101, ≈15× worse than BLE and Wi-Fi

Bill of materials

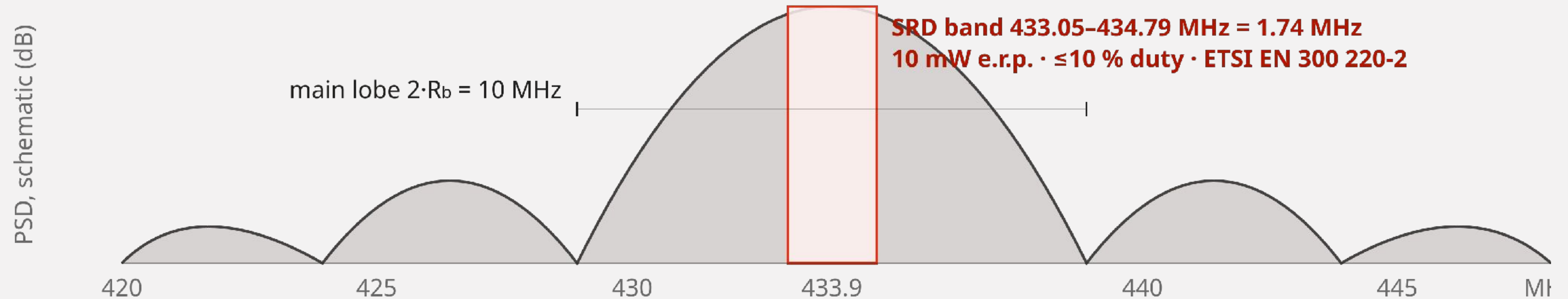
ITEM	QTY	NOTE	COST
BSS138AKW-Q MOSFET, SOT323	11	7 multiplier / driver, 4 bridge	
Inductors, SMD	34	350 pH – 98 nH	
Capacitors, SMD	40	1.4 pF – 1 μF	
Resistors, SMD	34	bias, pads, gate drive	
Subtotal: FETs and passives	119		\$0.67
Transformer, 1:1	1	modulator	\$0.30
Total, transmit path	120	parts only. without PCB, antenna or MCU.	\$0.97

Transmit path only, 120 components.
Excludes any PCB, antenna, MCU and connectors. Prices: single-unit distributor quotes

Limitations

01	No hardware	Circuit simulation only
02	Model validity	Switching-FET model: $t_{d(off)} \approx 10\text{ ns}$, $C_{iss} \approx 40\text{ pF}$ vs a 2.3 ns carrier period. indicative only.
03	Spectrum legality	$\approx 10\text{ MHz}$ main lobe; the 433 MHz SRD band is 1.74 MHz wide (10 mW e.r.p., 10 % duty). Lab-only.
04	Phase noise	PIO jitter reaches the carrier.
05	Efficiency	$\approx 0.5\text{-}1.5\%$ DC $\rightarrow$ RF: seven biased stages draw $\approx 1.2\text{ W}$ to deliver $\approx 6\text{ mW}$
06	Transmit only	No receiver: no closed link or BER. the demodulated data is an ideal correlator.

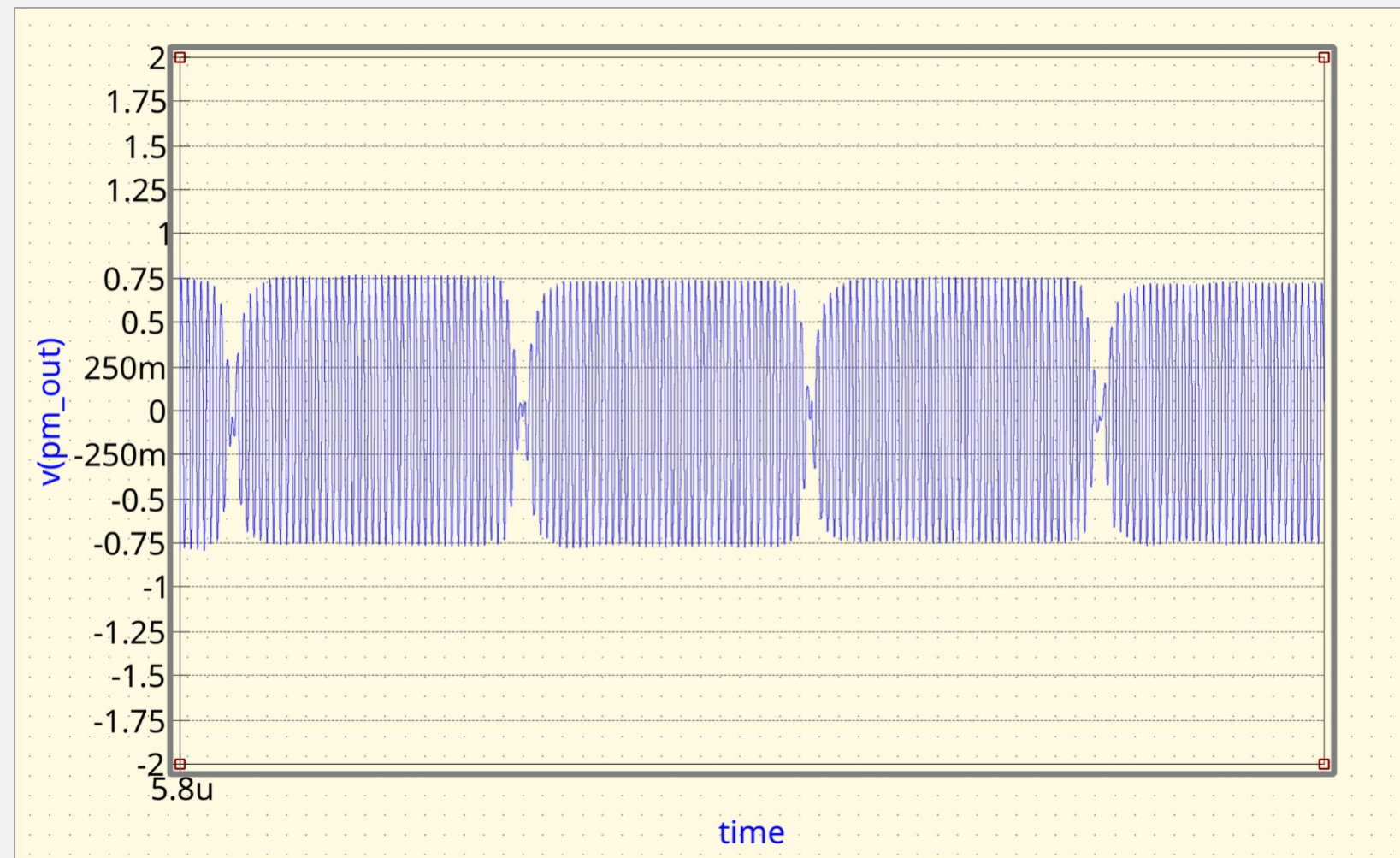
Band occupancy 10 MHz signal, 1.74 MHz band



Unfiltered BPSK at $R_b \approx 5$ Mbit/s occupies ≈ 10 MHz, nearly six times the allocation it sits in.

Phase flip at the symbol boundary

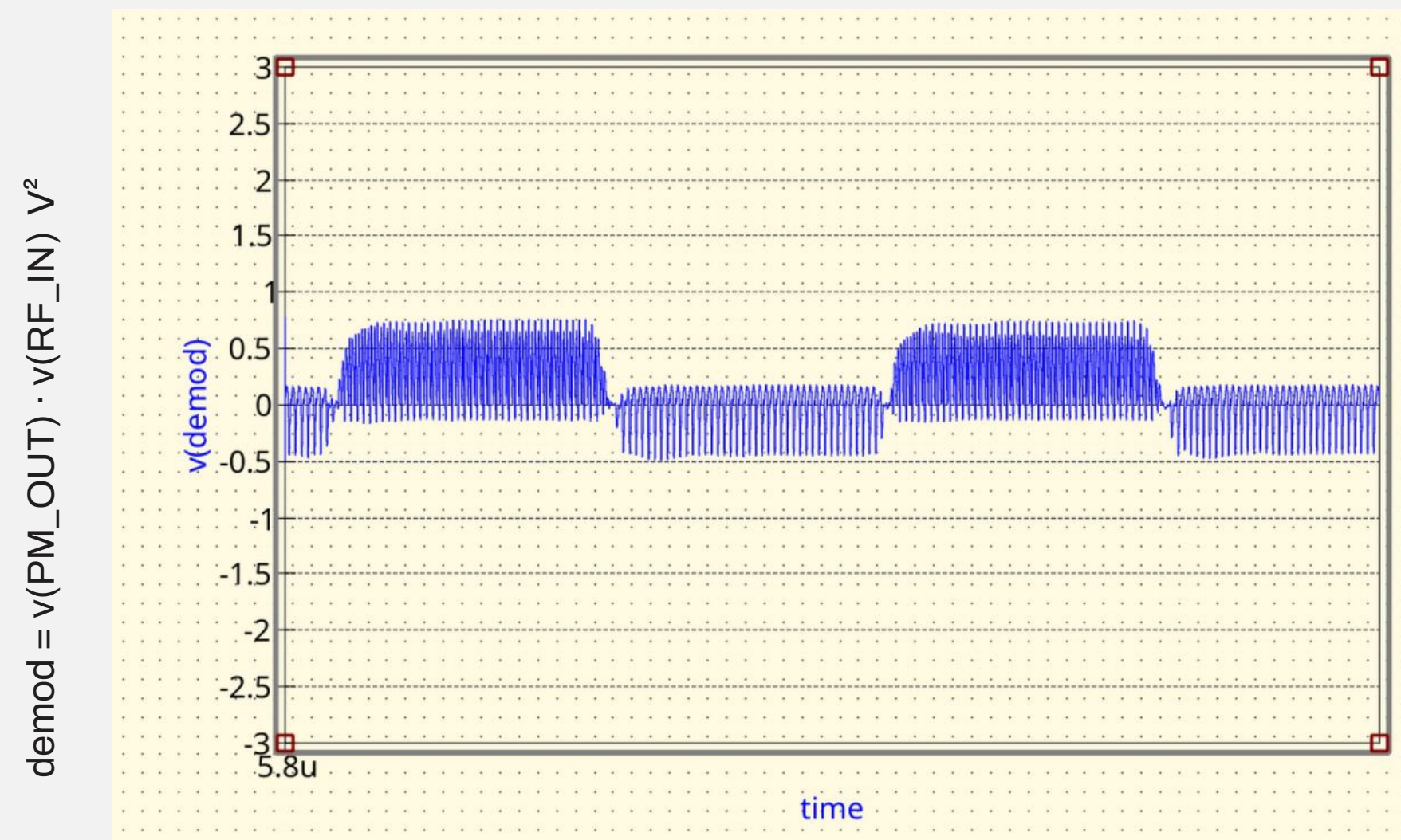
Output voltage across the 50 Ω load, v(PM_OUT) volts



Time window starts at 5.8 μ s; each flat segment is one 100 ns symbol, $\approx 0.5 \mu$ s shown

The carrier reverses sign at every symbol boundary: the envelope notch is the bridge switching pairs; on either side the 433.9 MHz carrier has opposite polarity BPSK. ± 0.75 V peak into 50 $\Omega \approx 5.6$ mW average ($\approx +7.5$ dBm).

Simulating demodulator

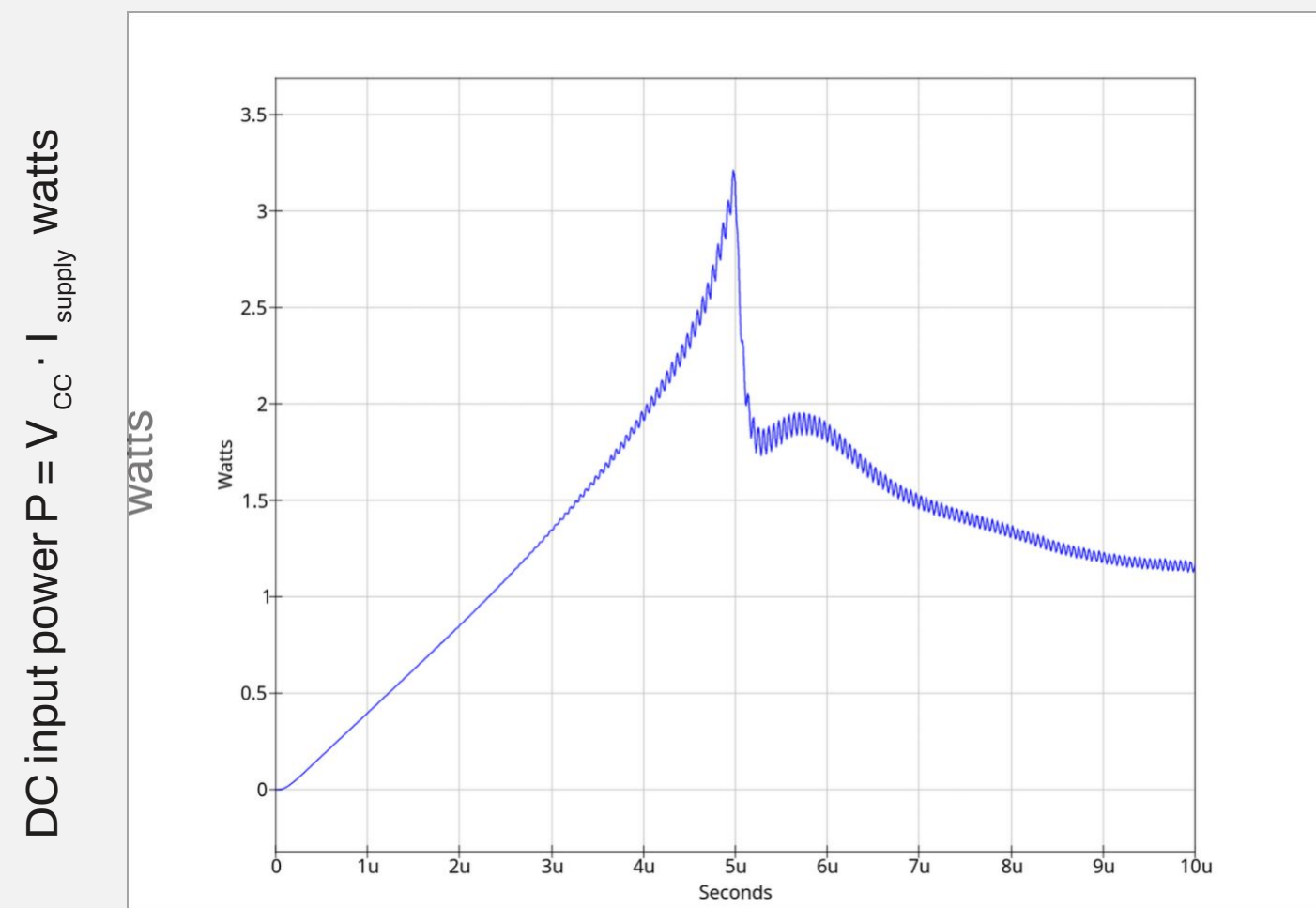


Time window starts at 5.8 μs ; each envelope segment is one 100 ns symbol (TR1 run)

The sign of the product is the bit

Multiplying the output by the unmodulated carrier $v(\text{RF_IN})$ taken before the bridge gives a product whose polarity follows the data proof that the polarity reversal is clean.

DC input power over the transient



Time, μs 0 to 10 μs (TR1 run). supply ramps 0 $\rightarrow$ 3.3 V over the first 5 μs

≈ 1.2 W in, ≈ 6 mW out

The 3.2 W peak is the 0 $\rightarrow$ 3.3 V supply ramp charging tanks and bias networks, not steady state. At 10 μs the power is ≈ 1.15 W and still settling.

Efficiency ≈ 5.6 mW / 1.2 W ≈ 0.5 %. Evenly shared, ≈ 0.11 W per SOT323 device. The driver stages carry most of it.

Future work

Build and measure

Lay out the board, build it, and measure spectrum, output power, harmonic suppression and distance.

Efficiency

At 1.2 W in for 15 mW out, most of the power goes into the multiplier chain rather than the antenna.

Close the link

A matching receiver to recover the suppressed carrier.

Band and rate

Retune to a band that fits the bandwidth or trade rate for compliance.

Model vs measurement

Quantify how far the switching FET SPICE model departs from reality at 433 MHz

Modulation and coding

The same four FET bridge can do QPSK by adding a quadrature path, doubling the rate at the same bandwidth.

Conclusion

We set out to move megabits between two microcontrollers below 1 GHz and in simulation the circuit does it. Eleven generic switching FETs and a handful of passives take an 18 MHz PIO clock to a 433 MHz BPSK carrier at 5 Mbit/s, with the CPU idle the whole time. The full transmit path simulates end to end, from the PIO clock to the modulated output into 50 ohms.

Sources

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Binary Phase ShiftKeying (BPSK)ModulationVersion 2 ECE IIT, Kharagpur
[https://www.idc-online.com/technical_references/pdfs/electronic_engineering/Binary_Phase_Shift_Keying_\(BPSK\)_Modulation.pdf](https://www.idc-online.com/technical_references/pdfs/electronic_engineering/Binary_Phase_Shift_Keying_(BPSK)_Modulation.pdf)

Nordic, nRF24L01+ Product Specification v1.0	nRF24L01+
Nordic, nRF52840 Product Specification	nRF52840 (BLE)
Espressif, ESP32-C3 Series Datasheet v1.7	ESP32-C3 (Wi-Fi)
Texas Instruments, CC1101 datasheet SWRS061	CC1101
Semtech, SX1276/77/78/79 Datasheet Rev. 7	SX1276 (LoRa)
ETSI EN 300 220-2 V3.2.1, Annex B	433 MHz band

Thank you!

The simulation is open on the laptop; we are happy to show any node or re-run anything after the session.