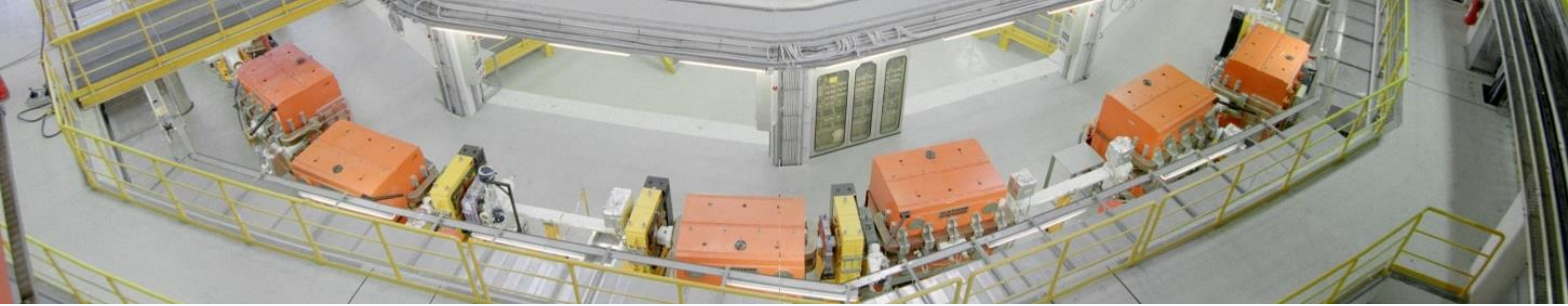


FPGA based detection of recombination rates during electron cooling

Mathis Beyß

Table of Content

FPGA = Field-programmable-Gate-Array

Integrated Circuit…

that can be configured after manufacturing.	that is based around a matrix of configurable logic blocks.
Field-programmable	**Gate-Array**

FPGAs are becoming famous …

The Rise of Programmable Network Hardware

It's becoming increasingly viable for enterprises to customize network hardware solutions.

SCI-TECH

Microsoft's Project Brainwave brings fast-chip smarts to AI at Build conference

Microsoft promises fast and flexible FPGA chips will unlock new AI abilities for customers using its Azure cloud-computing service.

BY STEPHEN SHANKLAND | MAY 7, 2018 6:41 AM PDT

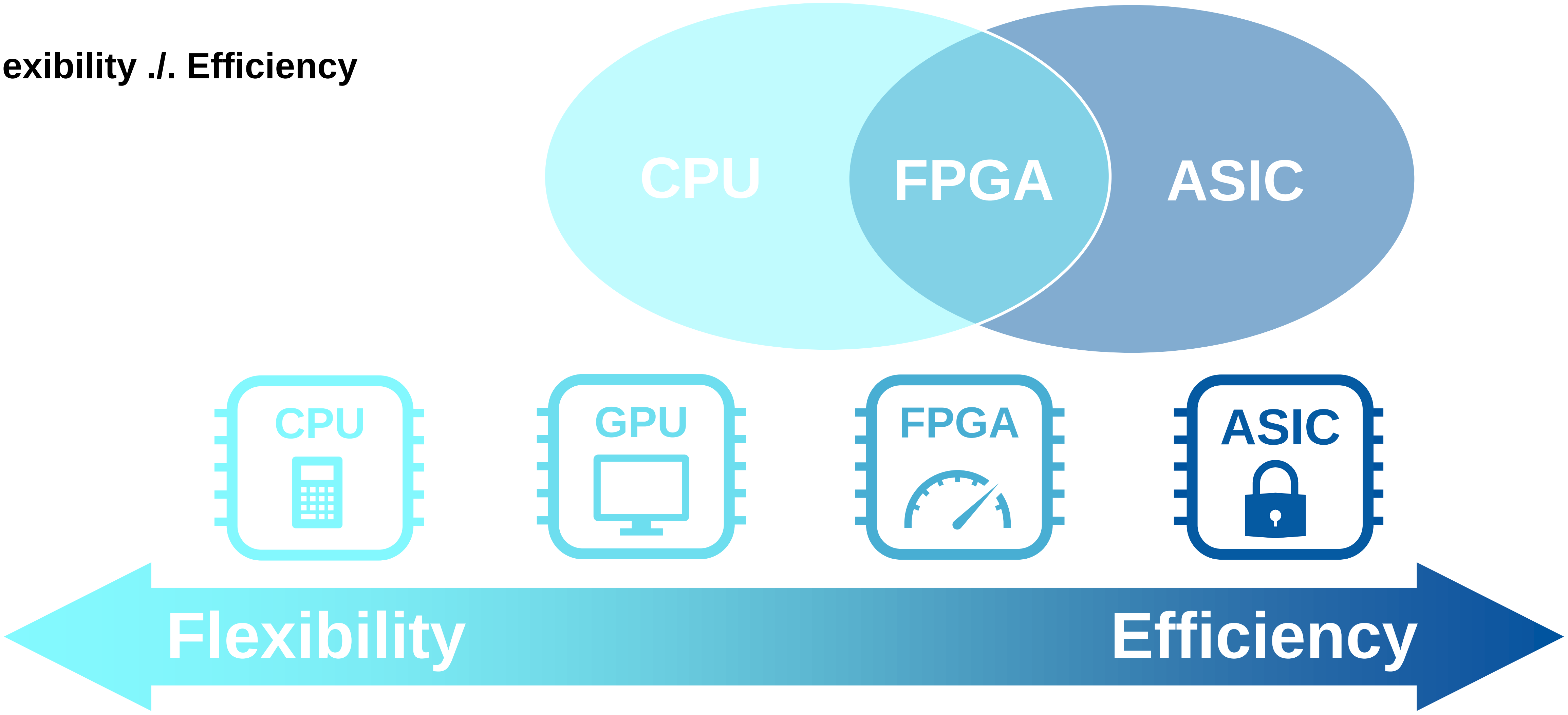
DESIGNLINES | AI & BIG DATA DESIGNLINE

Xilinx Buys China AI Startup

DeePhi acquisition seen as talent grab

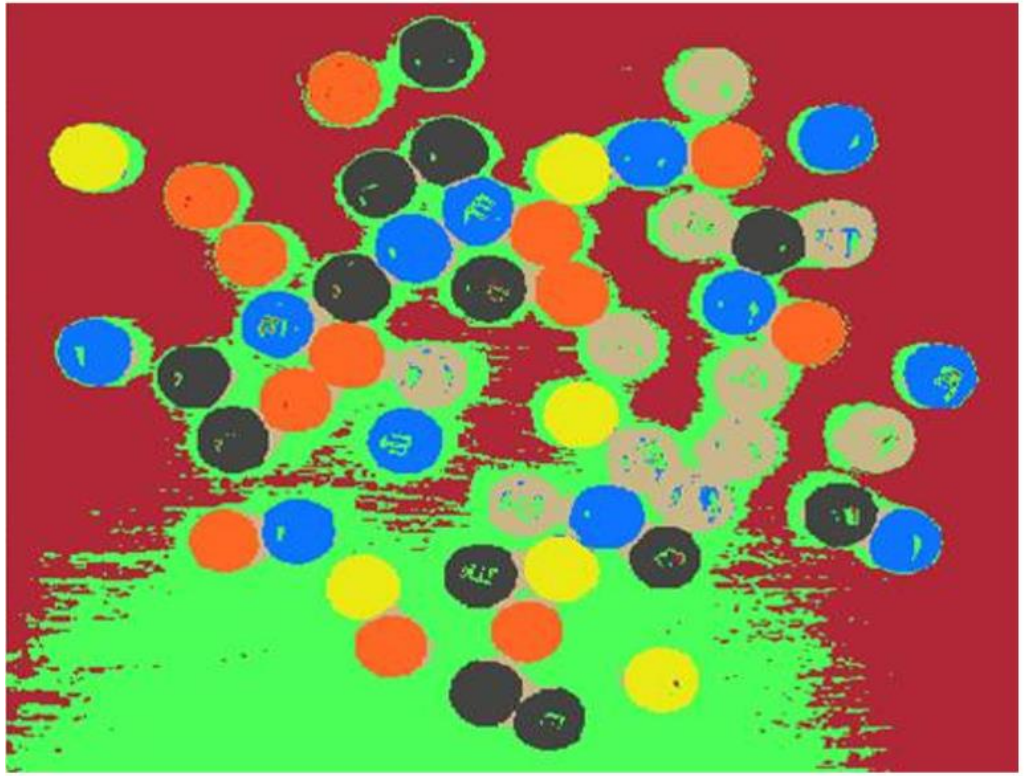
By Rick Merritt, 07.18.18 2

Flexibility ./. Efficiency



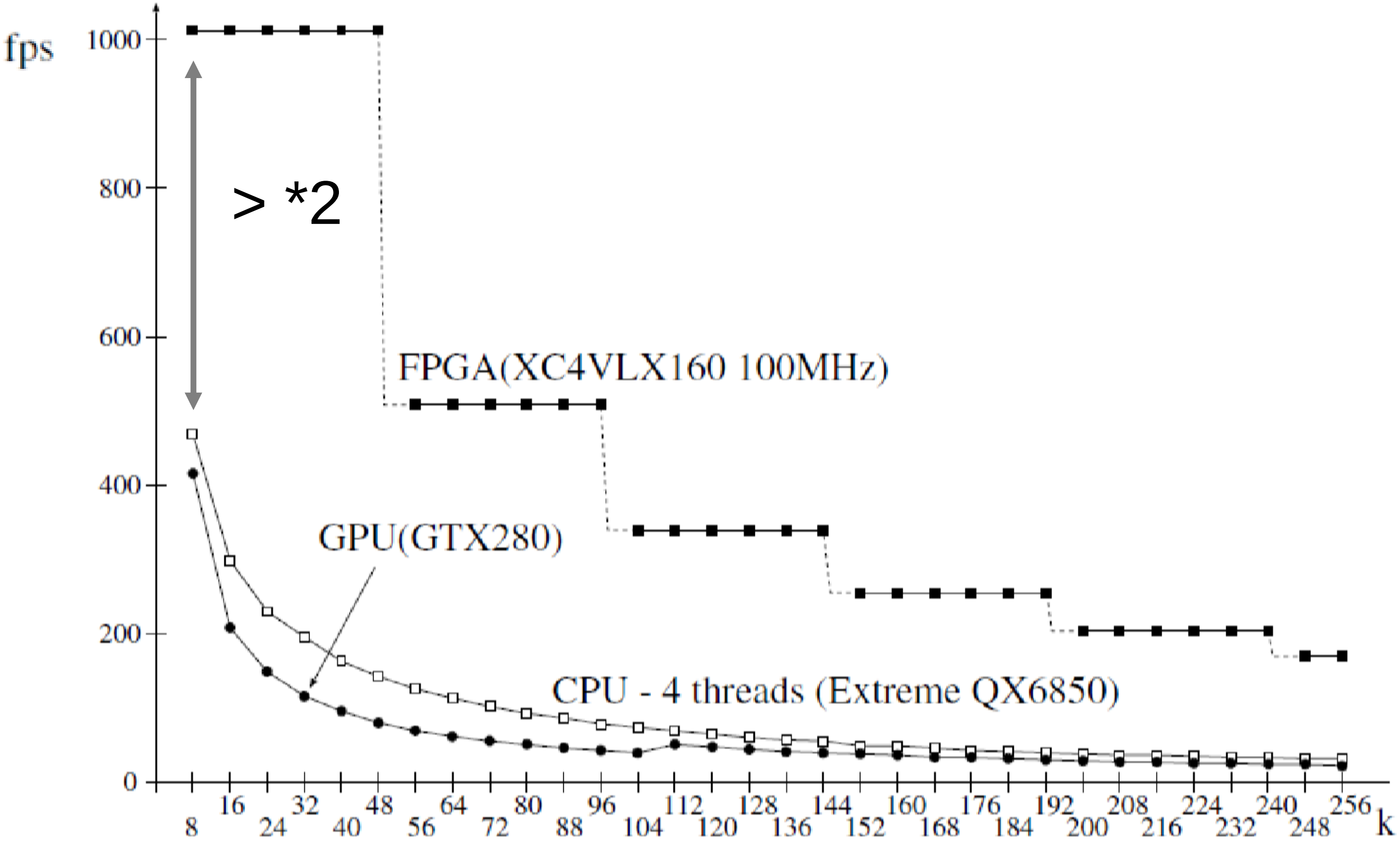
Example: Clustering M&Ms

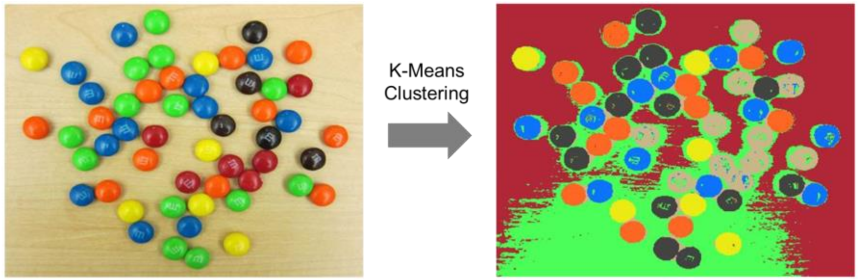
K-Means Clustering



Vortrag der TU-Dresden: Leistungsvergleich von FPGA, GPU und CPU für Algorithmen zur Bildbearbeitung

Example: Clustering M&Ms





[Vortrag der TU-Dresden: Leistungsvergleich von FPGA, GPU und CPU für Algorithmen zur Bildbearbeitung]

Comparison of different chip types

When to use FPGAs and when not?

- Parallel Processing
- Signal Processing
- Data-to-Clock-Ratios
- Deterministic I/O

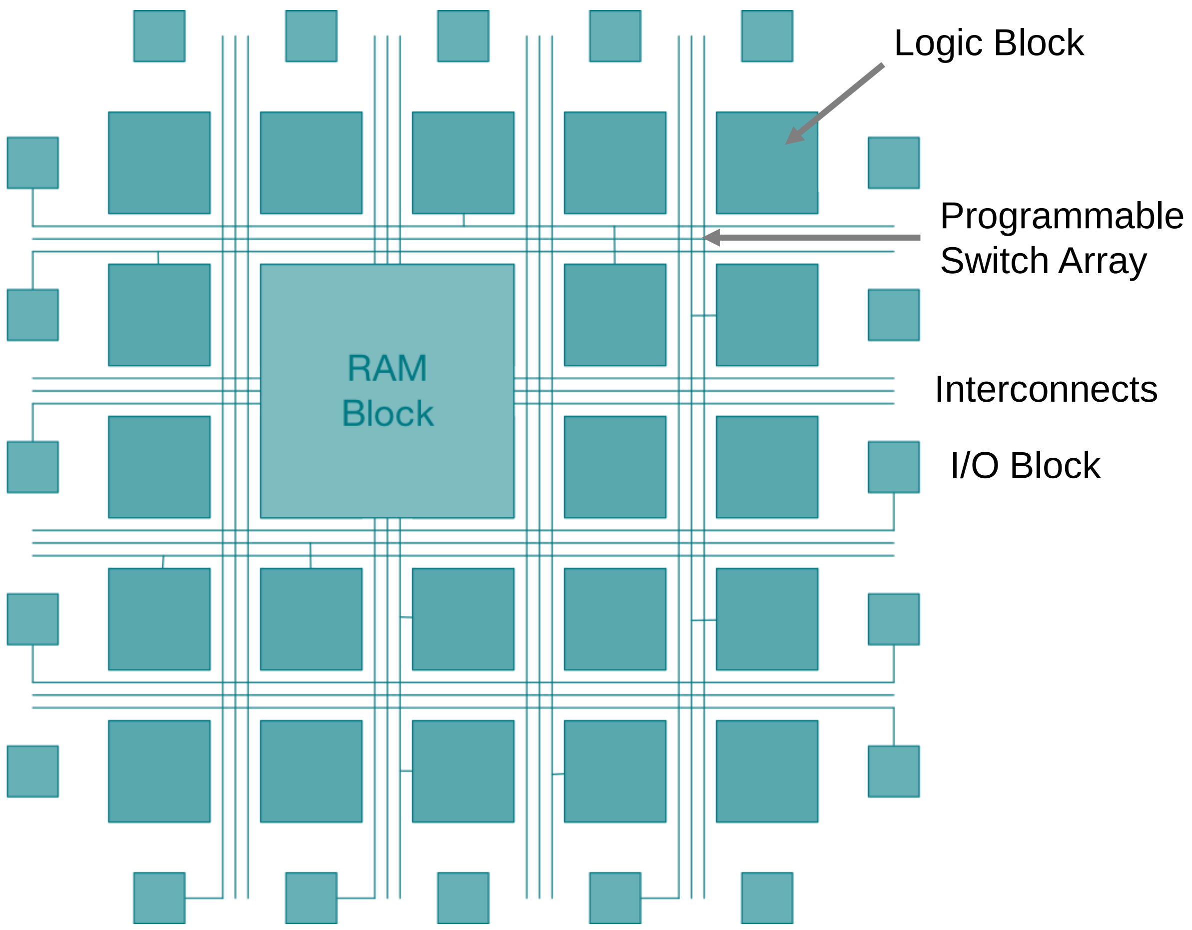
- Complex Calculations
- Floating Point Math
- Sorting & Searching

https://www.viewpointusa.com/IE/ar/when-is-an-fpga-worth-it-and-when-is-it-not-when-developing-an-industrial-embedded-system-part-1/

How do they work?

Main Parts of an FPGA Chip:

- Logic Blocks:
  - Look-Up Tables (LUTs)
  - Flipflops
- Programmable Switches
- Interconnects
- Random-Access Memory (RAM)
- I/O Blocks



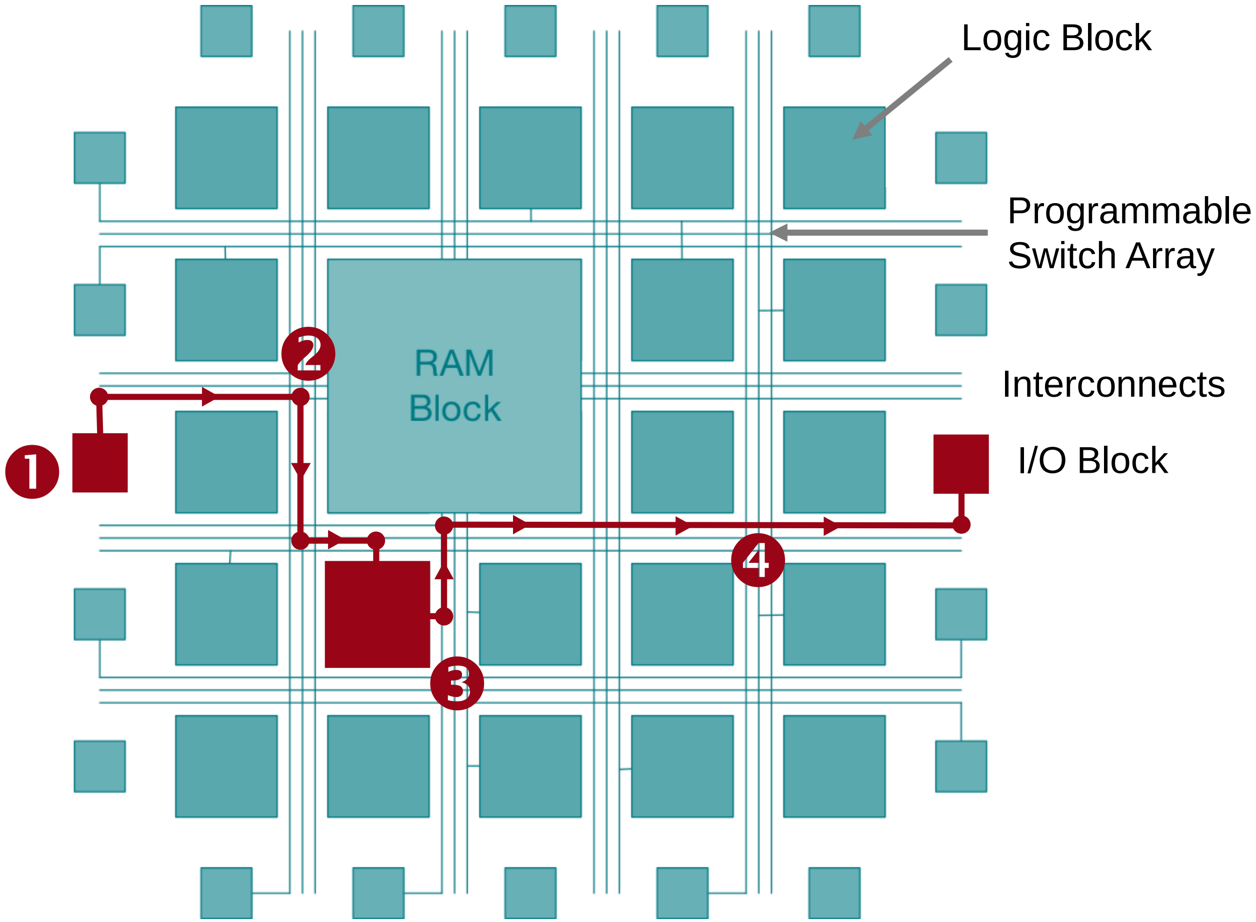
FPGA Working Principle

How do they work?

Basic Working Principle:

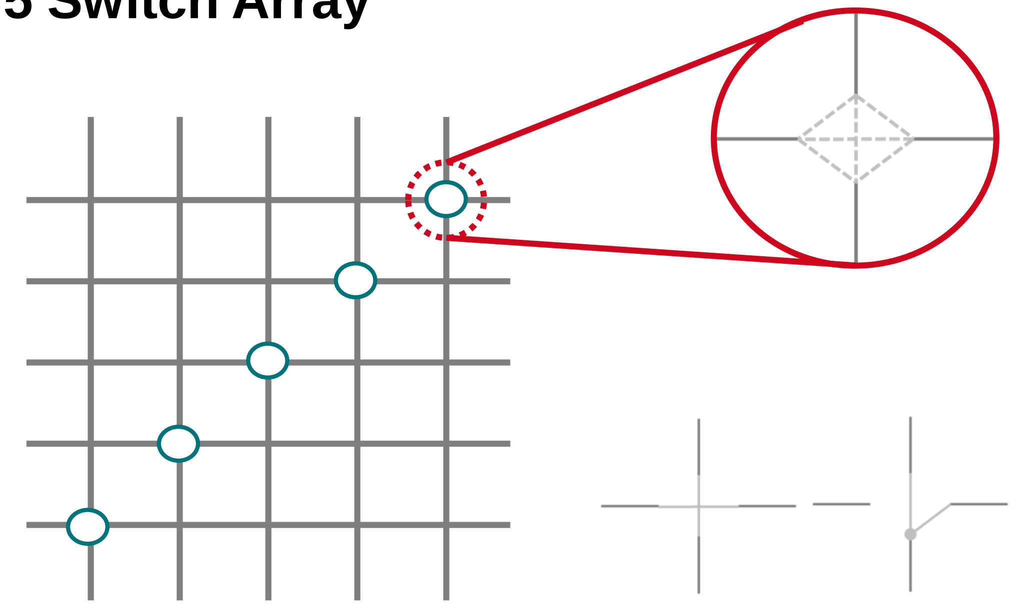
Signals are …

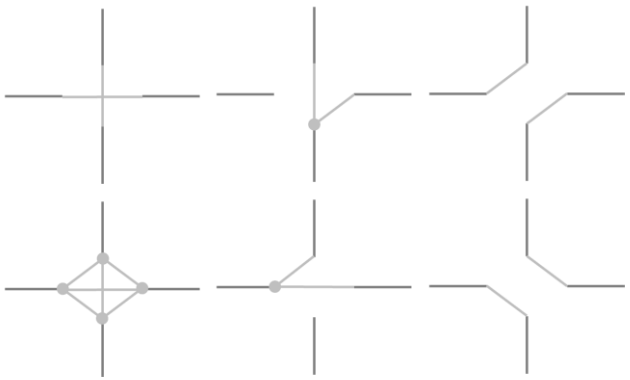
1) integrated via **Input Blocks**
2) routed via **Programmable Switches** to a certain Logic Block
3) processed in **Logic Block**
4) routed to **Ouput Block**



Programmable Switch Blocks

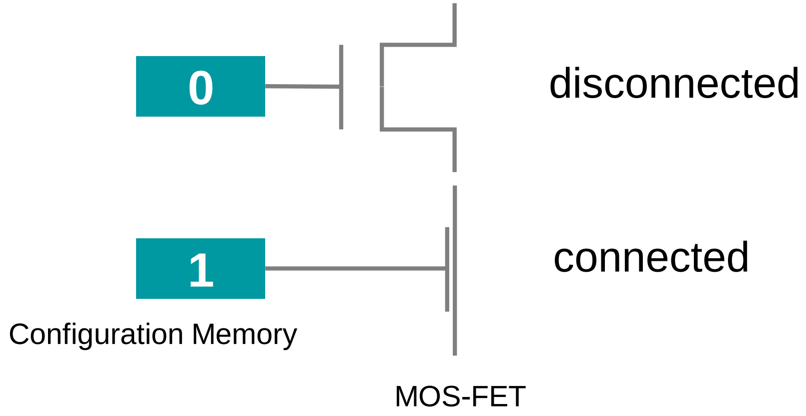
5×5 Switch Array





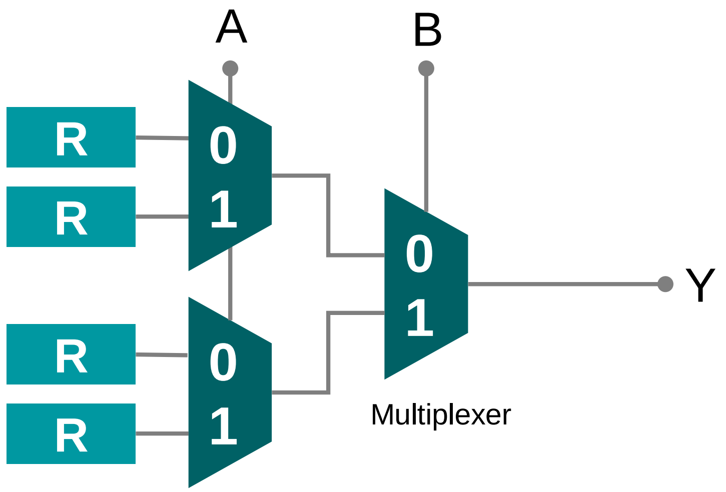
How are Programmable Switches implemented?

Each Crossbar consists of six Transistors, whose state is written to a configuration memory cell.

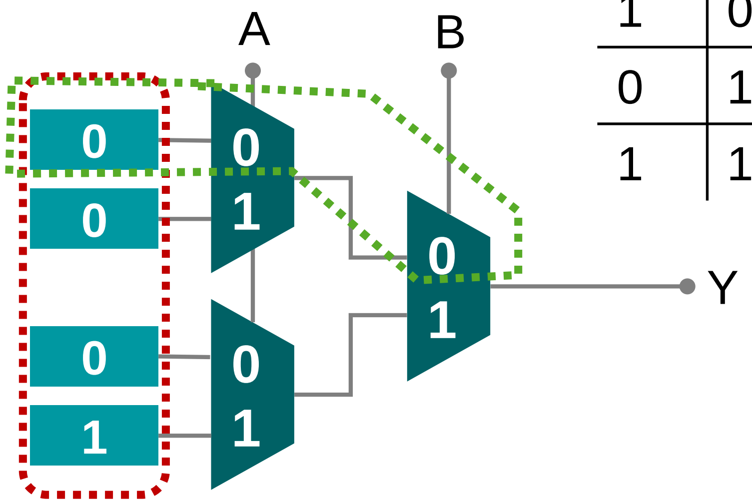


Look-Up Tables (LUTs)

2-Input LUT



Example – AND-Gate

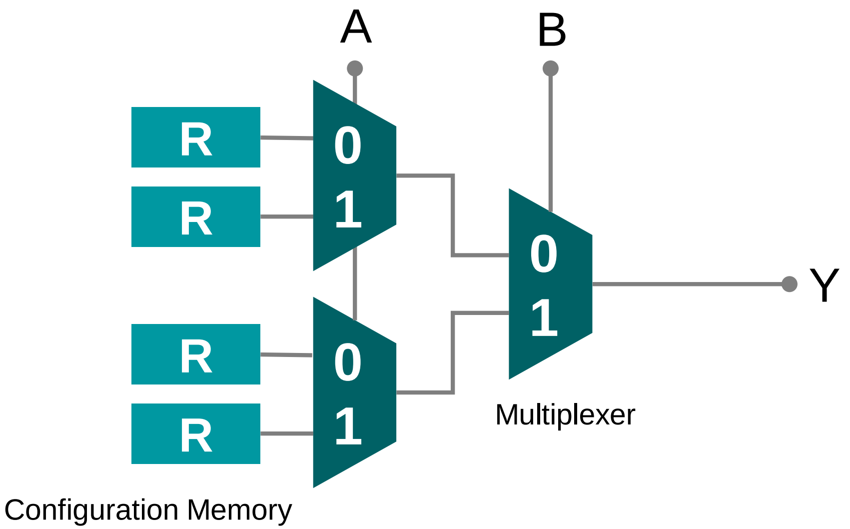


A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

- Every possible n-Input logic operation can be implemented within a n-Input LUT
- Modern FPGAs use blocks of 6-Input LUTs

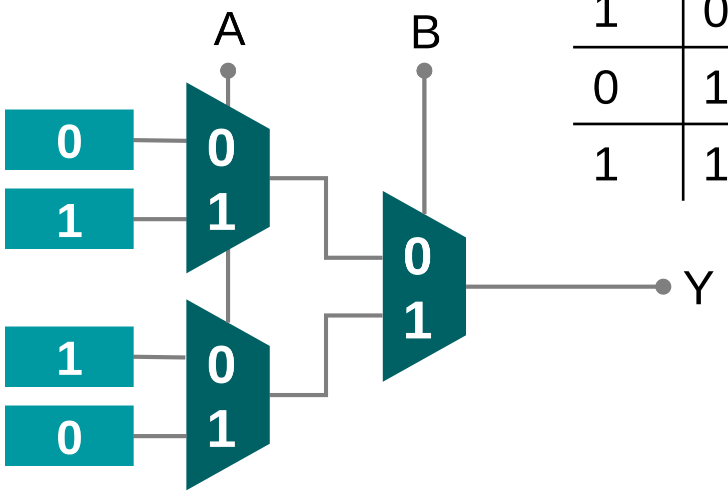
Look-Up Tables (LUTs)

2-Input LUT



Example – XOR-Gate

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0



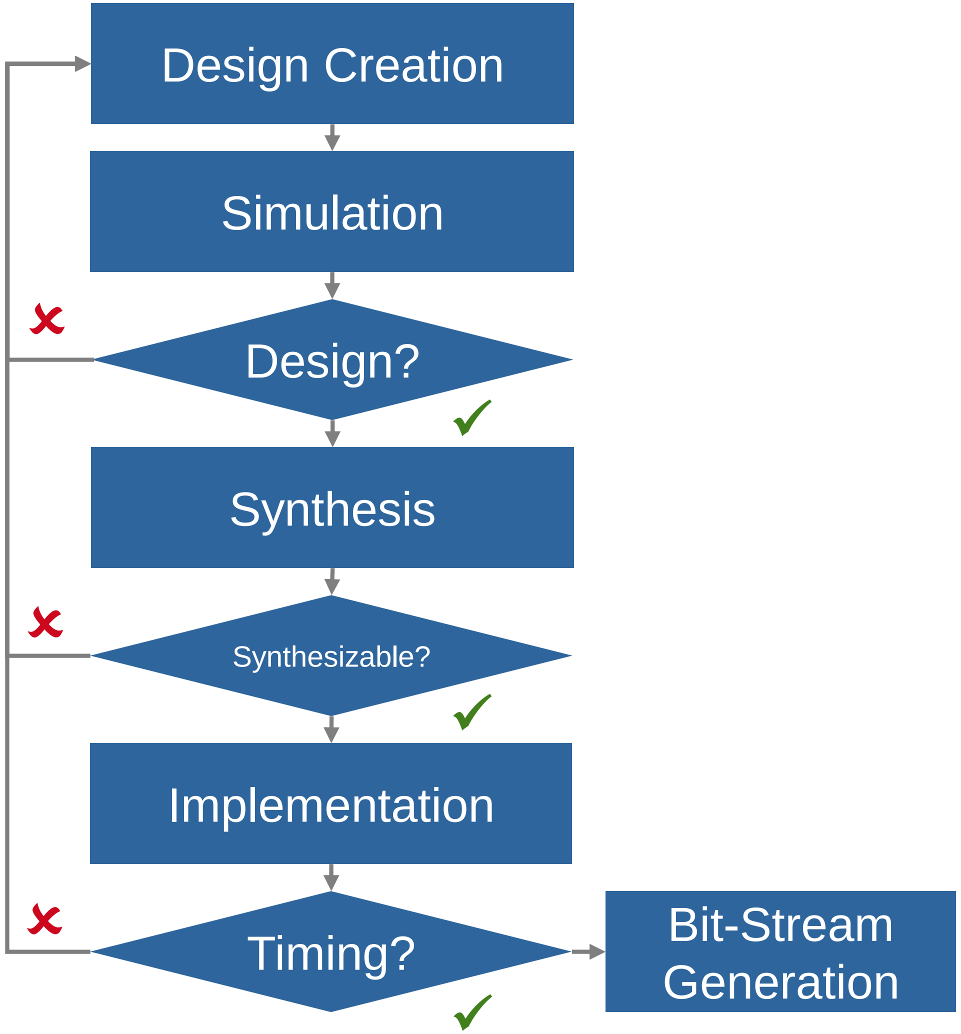
- Every possible n-Input logic operation can be implemented within a n-Input LUT
- Modern FPGAs use blocks of 6-Input LUTs

From the design to the configuration

Hardware Description Languages (HDL):

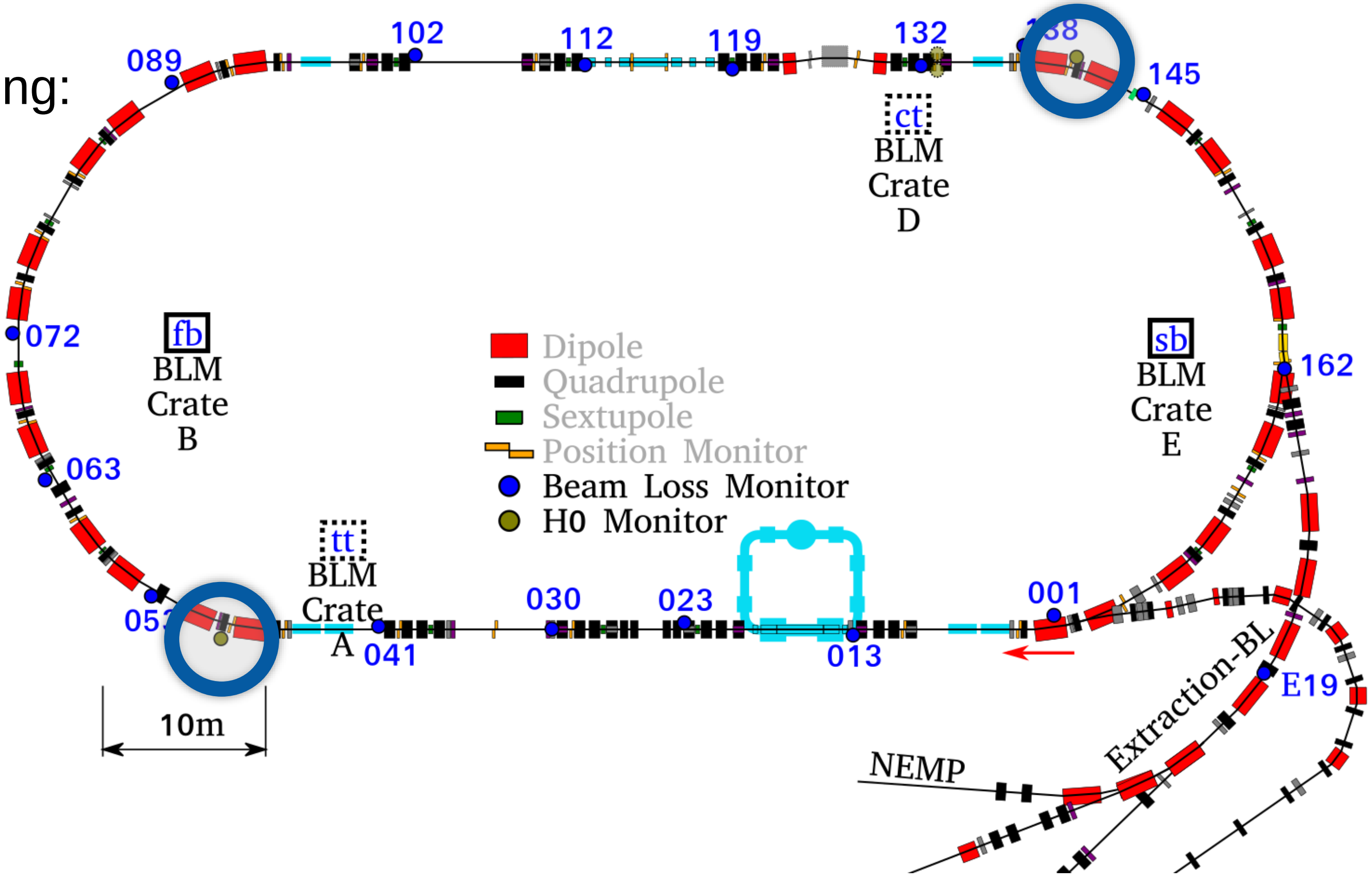
- **(System-)Verilog** (comparable to C)
- **VHDL** (comparable to Fortran)

Meanwhile it is also possible to use standard programming languages to synthesize FPGA Designs like Python (PYNQ, MyHDL) or MATLAB (HDL Coder & Verifier)

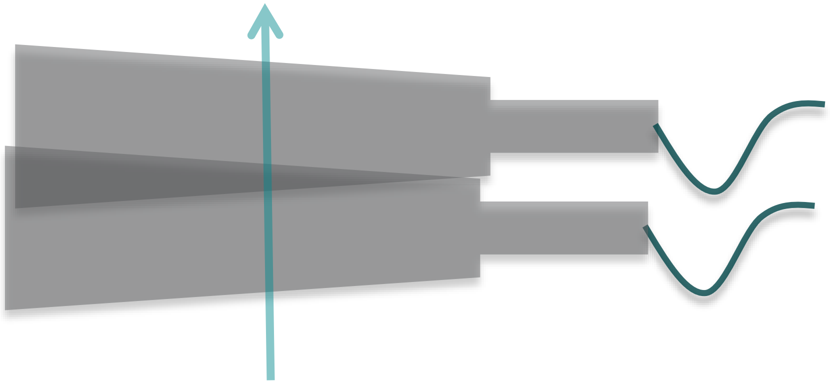


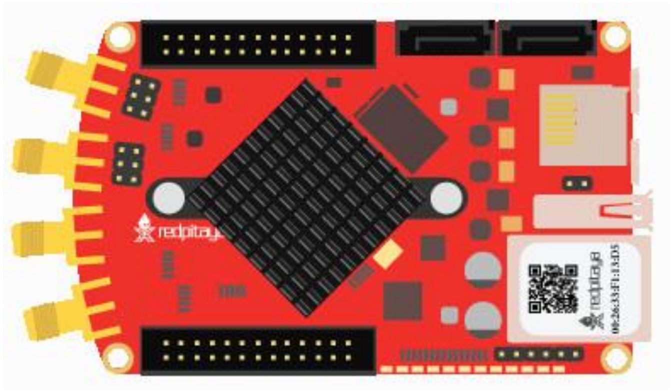
Beam Loss & H0 Monitoring

- 9 detectors for Beam Loss Monitoring:
  - 7 along the ring
  - 2 on the extraction beam line
- 2 detectors for H0 Monitoring:
  - 1 behind the 100keV Cooler
  - 1 behind the 2MeV Cooler



System-on-a-Chip Approach





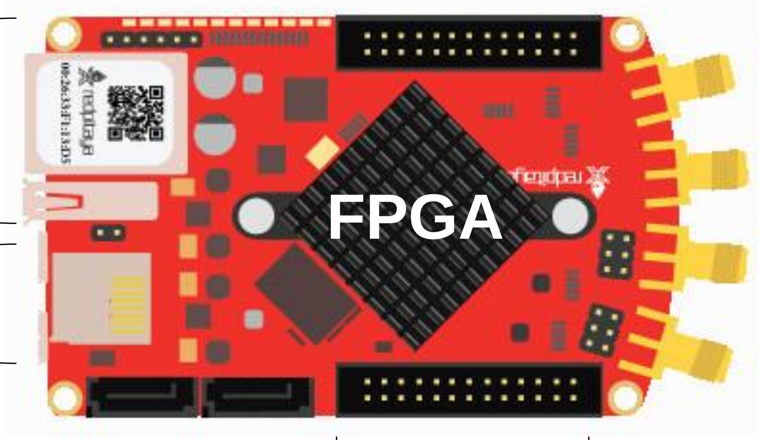
EPICS

Scintillator Paddles | **Development Board** | **Control System**

STEMlab 125-14

Ethernet/ USB Connection

SD Card with OS



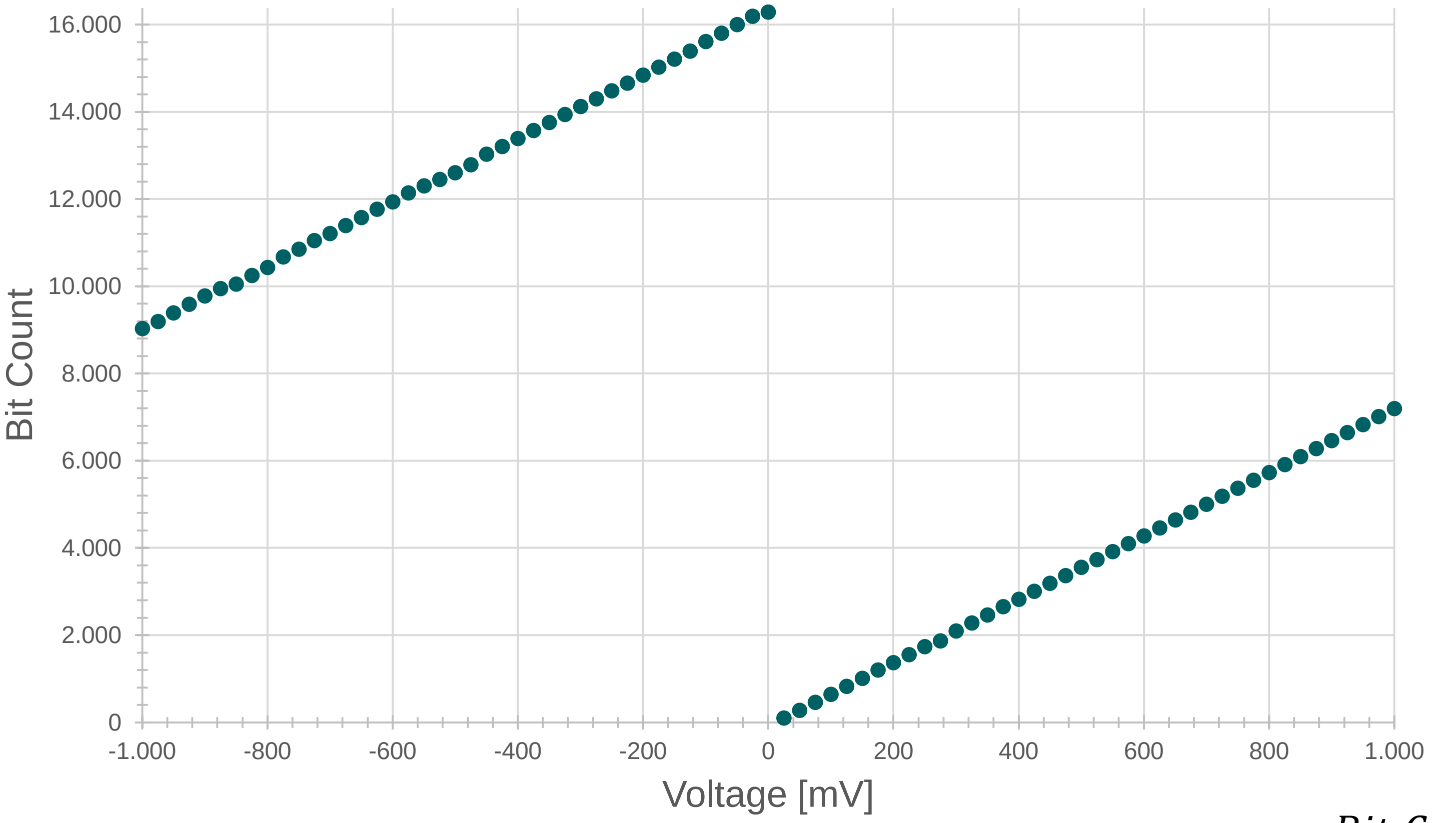
2 Analog IOs

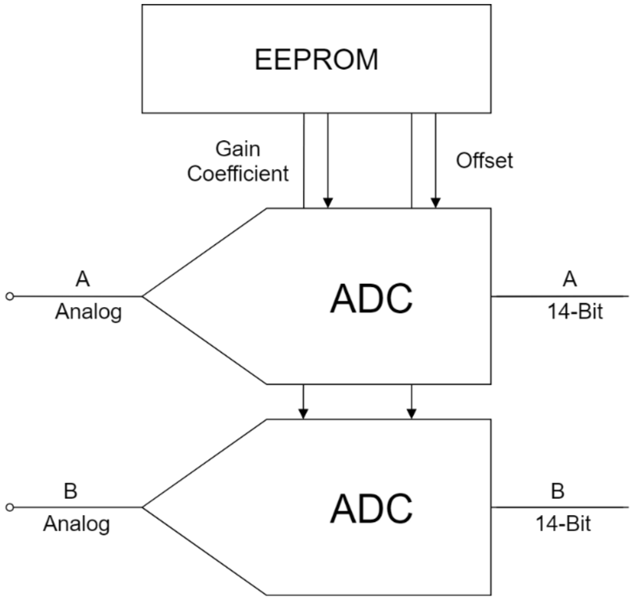
8 Digital IOs

Basic Specifications

- Xilinx ZYNQ 7010 SOC
  - Look-Up Tables: 17 600
  - Logic Cells: 28 000
  - Flip_Flops: 35 200
  - On-Chip RAM: 2.1 Mb
- 2 ADCs
  - Sample Rate: 125 MS/s
  - Resolution: 14 bit
  - Voltage range: ±1V (LV), ±20V (HV)

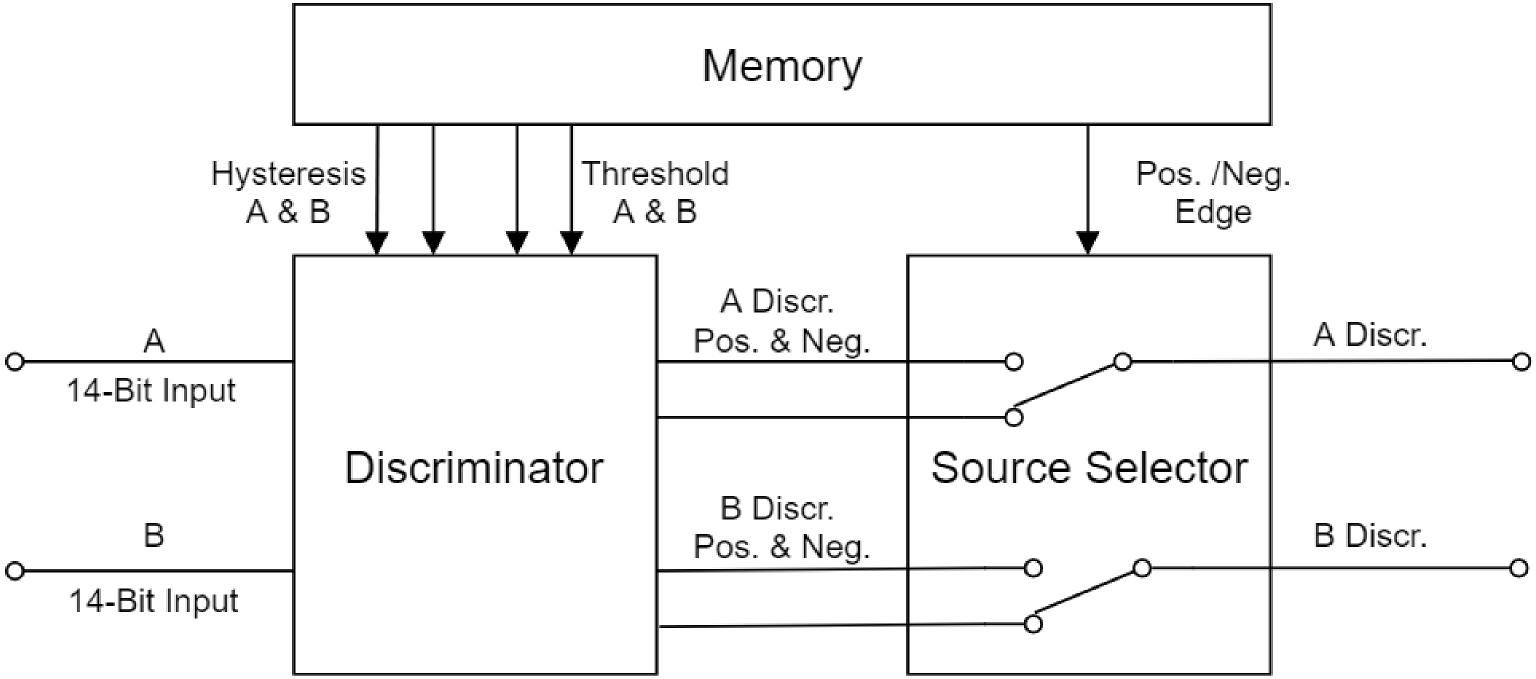
Analog-to-Digital-Conversion



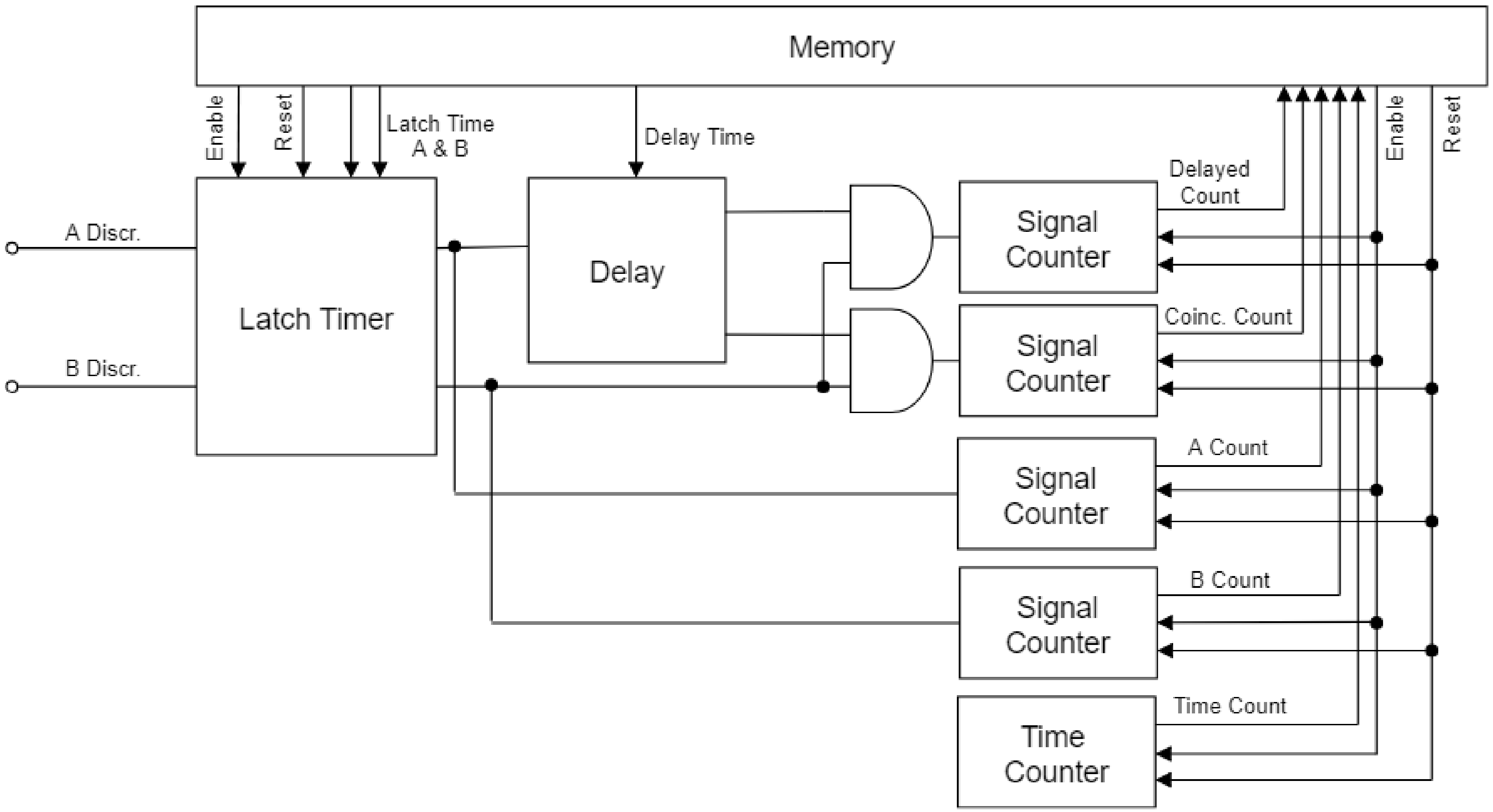


$$Bit\ Count = Gain\ Coefficient\ [1/V] \cdot Voltage\ [V] + Offset$$

Signal Preparation



Signal Processing



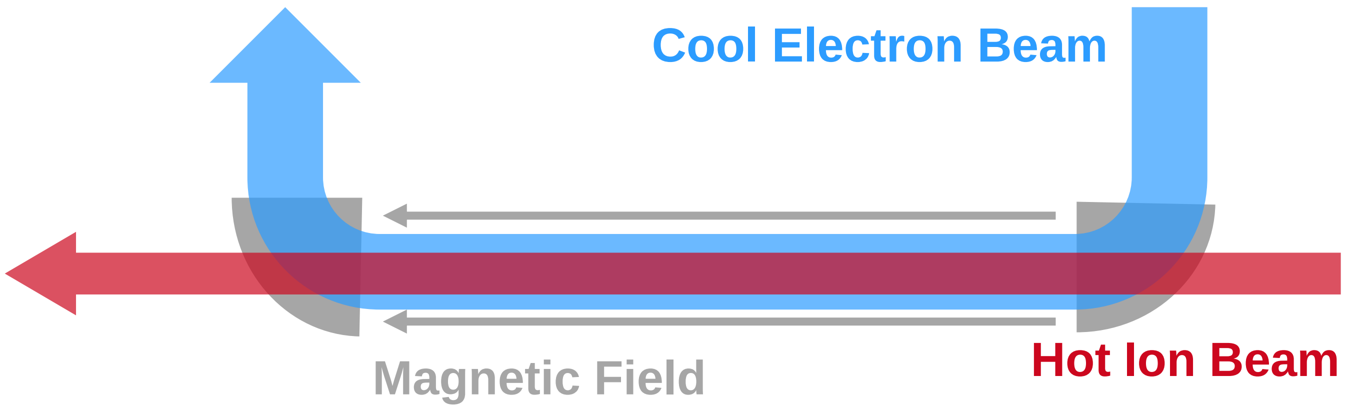
Basic working principle

- Superposition with quasi-monoenergetic dense electron beam with the same velocity
- Coulomb Scattering leads to a momentum transfer
- Thermal energy loss in the co-moving electron beam

$$\frac{E_i}{E_e} = \frac{m_i}{m_e}$$

→ 100 keV electron beam cools 1837 MeV proton beam

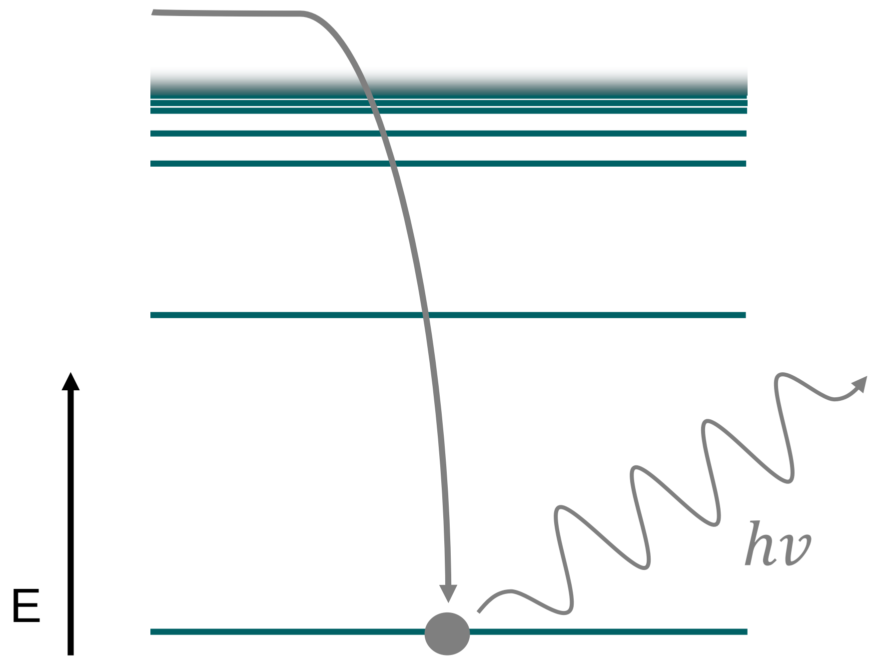
$$k_B T_\perp \approx 0.1\, eV$$
$$k_B T_{||} \approx 1\, meV$$



Recombination Processes

Radiative Recombination:

$$p^+ + \ e^- \ \rightarrow H^0 + h\nu$$



Typical recombination rate is on the order of several *kHz*

How to calculate the recombination rate?

Calculating the Recombination Rate

$$R = \gamma^{-1} \overbrace{\eta_L N_p}^{\text{Ions occupied by e-beam}} \underbrace{n_e \alpha_{RR}}_{\substack{\text{recombination} \\ \text{rate per Ion}}} \qquad \text{with } \alpha_{RR} = \langle v\sigma(E) \rangle$$

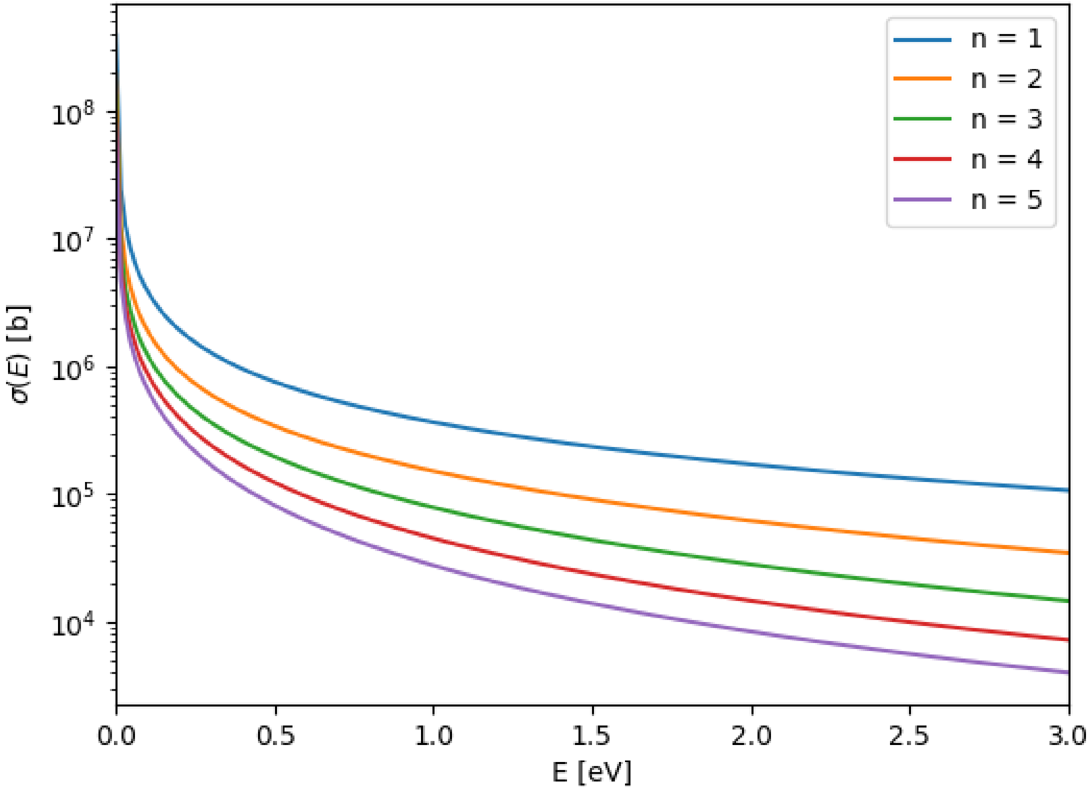
η_L	fraction of beam occupied by e-beam
N_p	number of protons in the beam
n_e	electron density in e-cooler
α_{RR}	recombination coefficient
v	relative velocity
$\sigma(E)$	cross-section

A. Wolf et Al.: Recombination in Electron Coolers

Kramers formula for radiative recombination

$$\sigma_n(E) = \frac{32\pi}{3\sqrt{3}} \alpha^3 a_B^2 \frac{q^4 R_\infty^2}{nE(q^2 R_\infty + n^2 E)}$$

α	fine structure constant
n	Rydberg level
q	ion charge
a_B	Bohr radius
R_∞	Rydberg energy
E	electron energy in ion resting frame

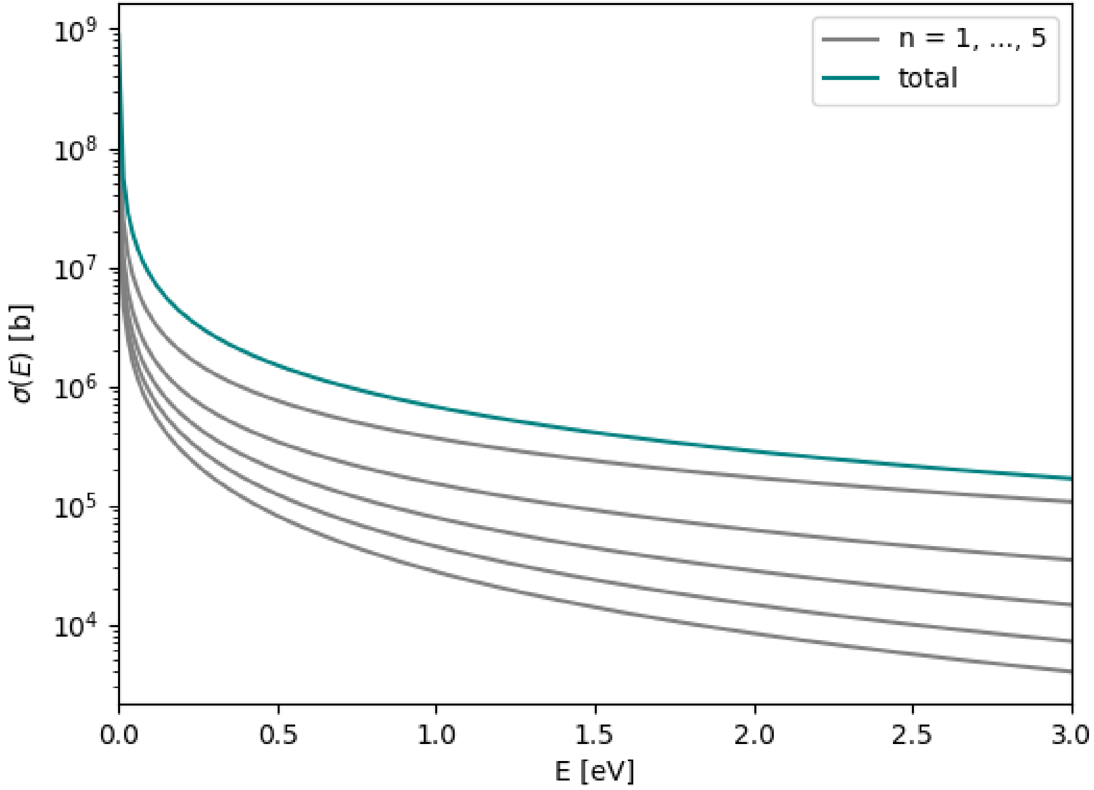


H. A. Kramers: On the theory of X-ray absorption and of the continuous X-ray spectrum

Calculation of the total Cross Section

$$\sigma_n(E) = \frac{32\pi}{3\sqrt{3}}\alpha^3 a_B^2 \frac{q^4 R_\infty^2}{nE(q^2 R_\infty + n^2 E)}$$

$$\sigma_{tot}(E) = \sum_{n=1}^{\infty} \sigma_n(E) \approx \sum_{n=1}^{n_{max}} \sigma_n(E)$$



A. Wolf et Al.: Recombination in Electron Coolers

Calculation of the total Cross Section

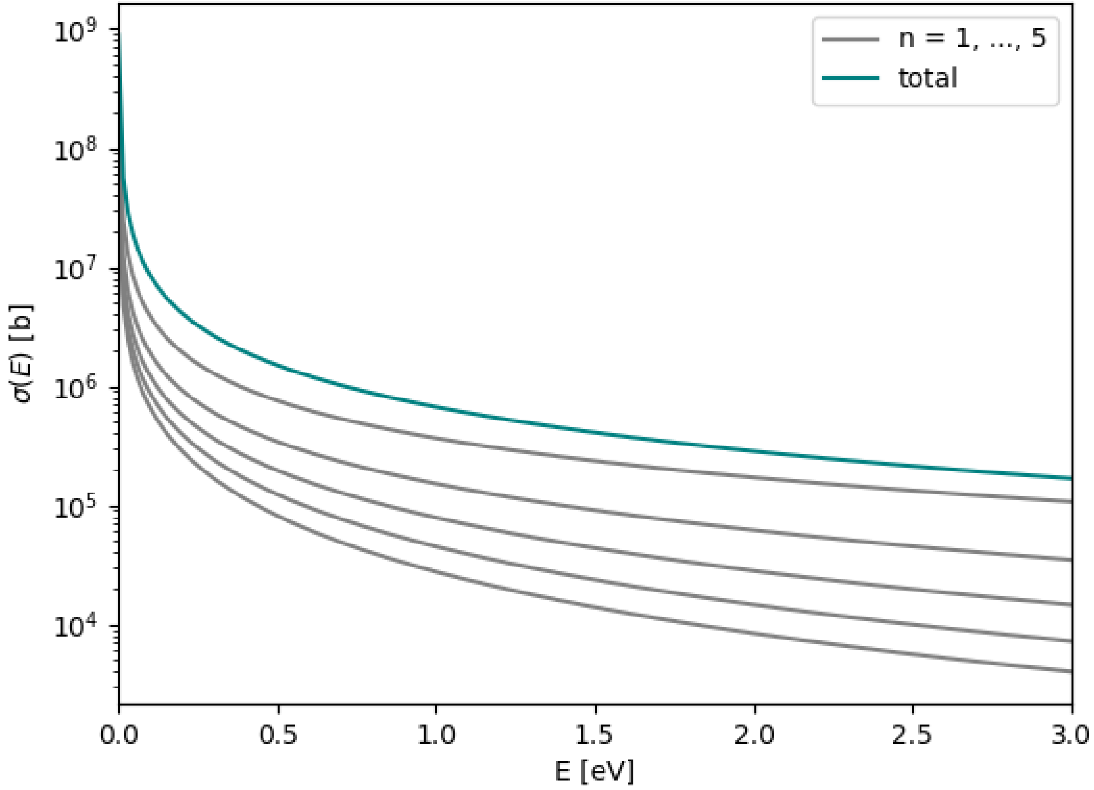
$$\sigma_n(E) = \frac{32\pi}{3\sqrt{3}}\alpha^3 a_B^2 \frac{q^4 R_\infty^2}{nE(q^2 R_\infty + n^2 E)}$$

$E \ll q^2 R_\infty$:

$$\sigma_{tot}(E) \approx \frac{32\pi}{3\sqrt{3}}\alpha^3 a_B^2 \theta^2 \left(\gamma + \ln(\theta)\right)$$

$$\gamma = 0.5772$$

$$\theta = \mathrm{q}\sqrt{R_\infty/E}$$



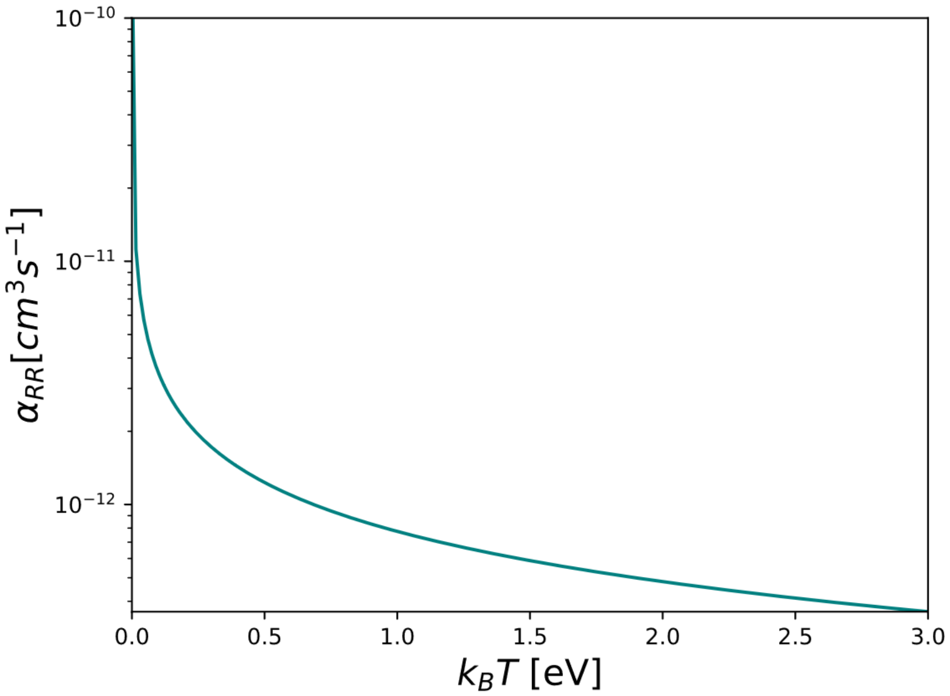
A. Wolf et Al.: Recombination in Electron Coolers

Calculation of the Recombination Coefficient

$$\alpha_{RR} = \langle v\sigma_{tot}(E)\rangle = \frac{\int_0^\infty dv\ v^2\sigma_{tot}(E)\, f(E)}{\int_0^\infty dv\, v\, f(E)}$$

with the “flattened“ Maxwell distribution:

$$f(E) = \frac{m_E}{2\pi k_B T} \cdot e^{-\frac{E}{k_B T}} \delta(V_{||})$$



$$\boxed{\alpha_{RR} = 3.02 \cdot 10^{-13}\,\frac{cm^3}{s} q^2 \sqrt{\frac{eV}{k_B T}}\left[ln\left(11.32 \cdot q\sqrt{\frac{eV}{k_B T}}\right) + 0.14 \cdot \sqrt[3]{\frac{k_B T}{q^2 eV}}\right]}$$

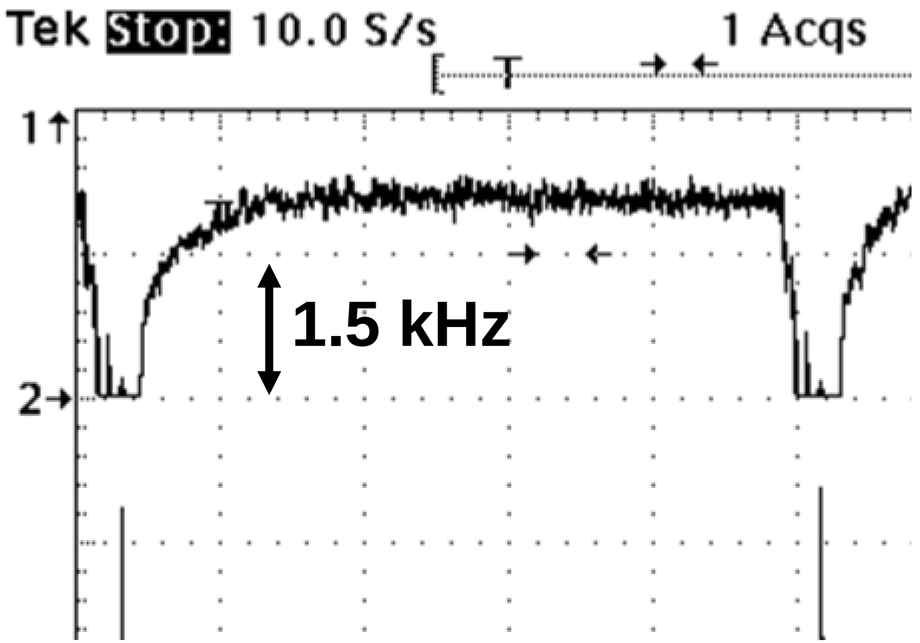
M. Bell and J. S. Bell: Capture of Cooling Electrons by cool Protons

Effective Temperature

Calculation of the effective temperature from Recombination Rates

$$\alpha_{RR} \approx 7.88\,(k_B T)^{-0.675} 10^{-13} \frac{cm^3}{s}$$ good approximation for $k_B T < 3\ eV$

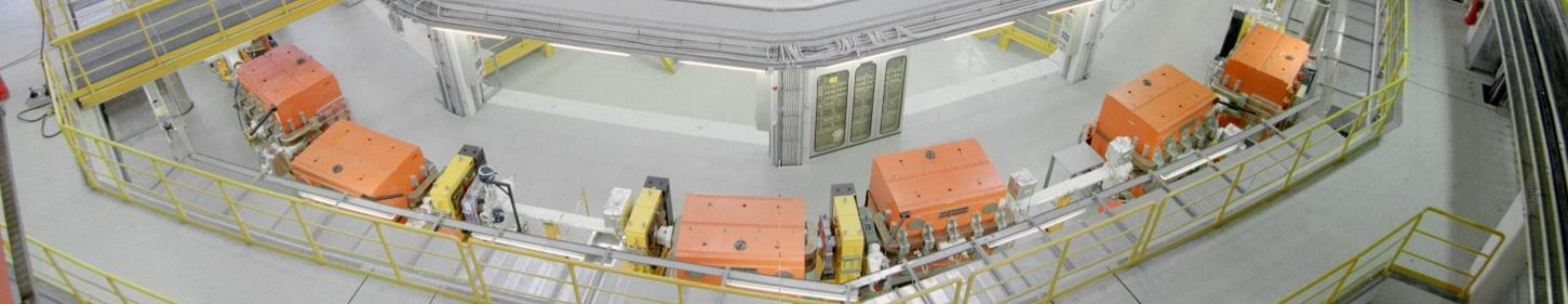
Stop cooling, when recombination rate reaches his maximum.
→ No more cooling, only beam loss



H. Poth et al.: First Results of Electron Cooling Experiments at LEAR

- FPGAs are configurable Integrated Circuits.
- They can be used for real-time signal processing.
- They are used at COSY for rate counting and charge integration.

- Electrons and ions can recombine during cooling.
- One can derive a theoretical formula for the recombination rate.
- One can use the recombination rate to gain insight into the cooling process



Thank you
for your attention!