3D-CHIP

TECHNOLOGY AND APPLICATIONS OF MINIATURIZATION

23.08.2018 I DAVID ARUTINOV

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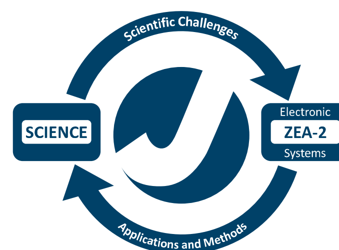

CONTENT

- INTRODUCTION
- TRENDS AND ISSUES OF MODERN IC's
- 3D INTEGRATION TECHNOLOGY
- CURRENT STATE OF 3D INTEGRATION
- SUMMARY

INTRODUCTION

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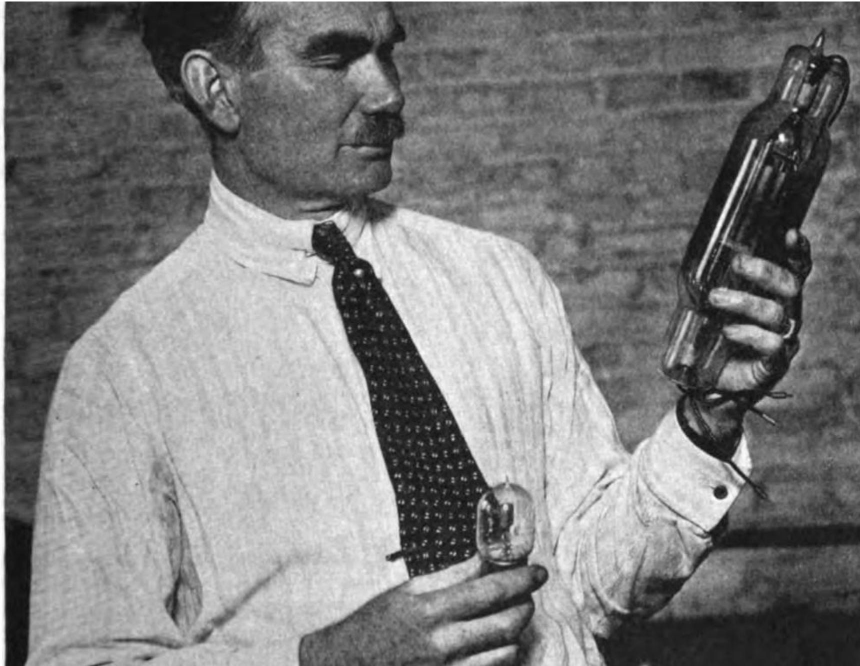
VACUUM TUBES



De Frost with a vacuume tube triode [2]. Around 1920.

A vacuum tube radio [12]. Around 1940.

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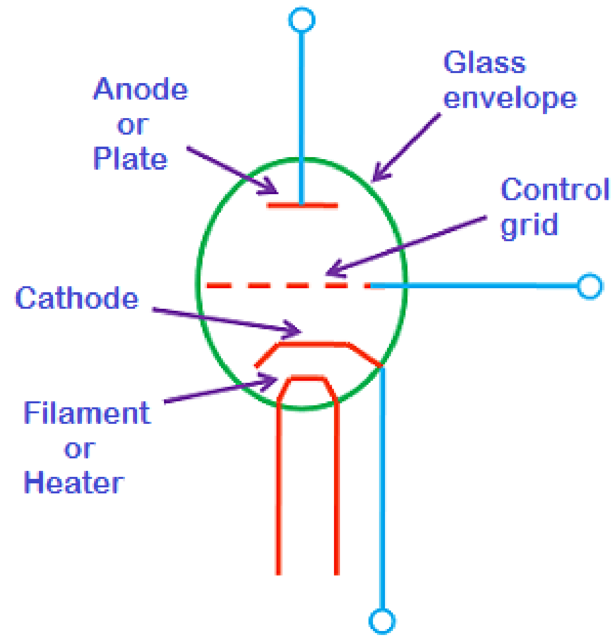
VACUUM TUBES



De Frost with a vacuume tube triode [2]. Around 1920.

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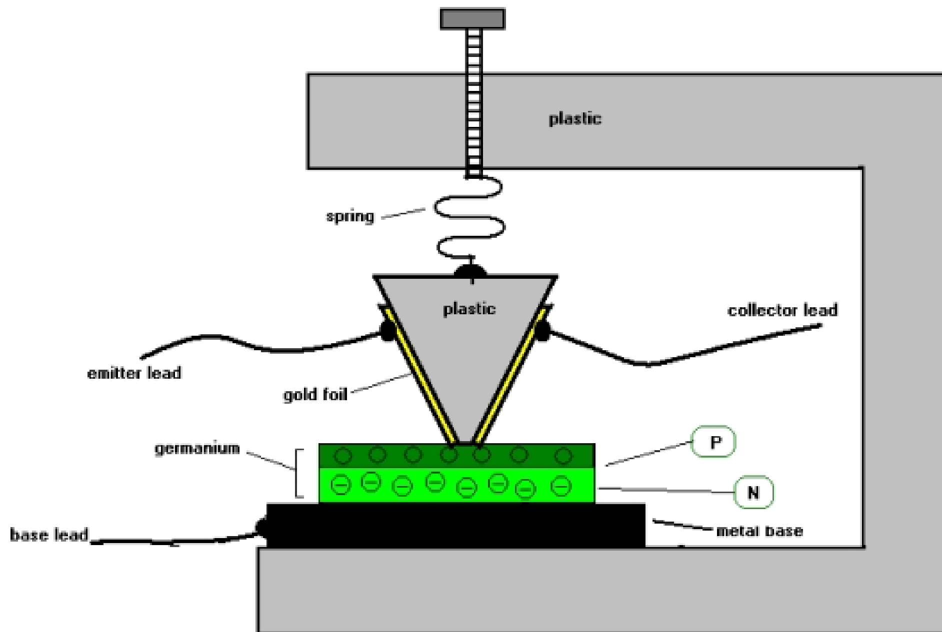
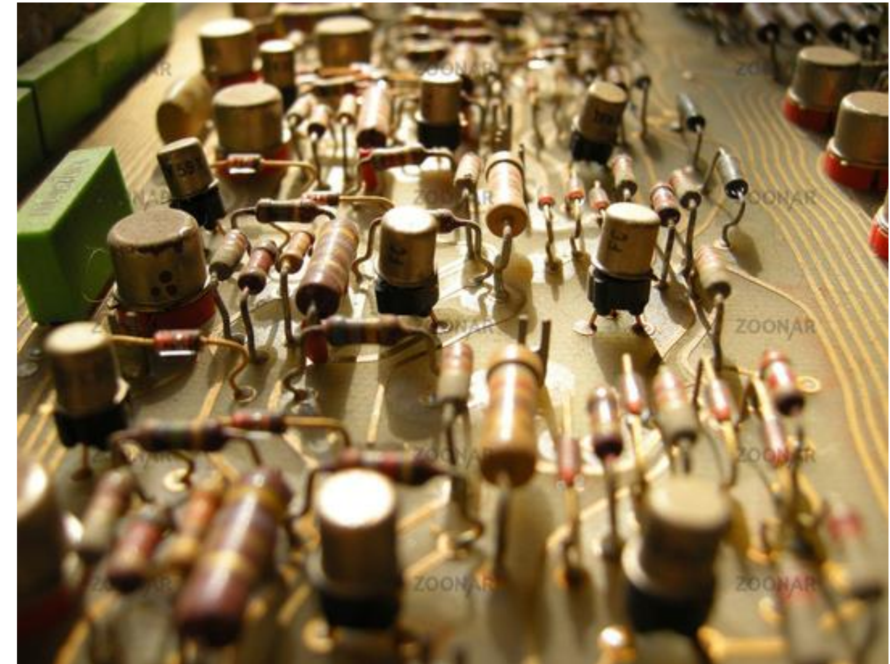
FIRST TRANSISTOR



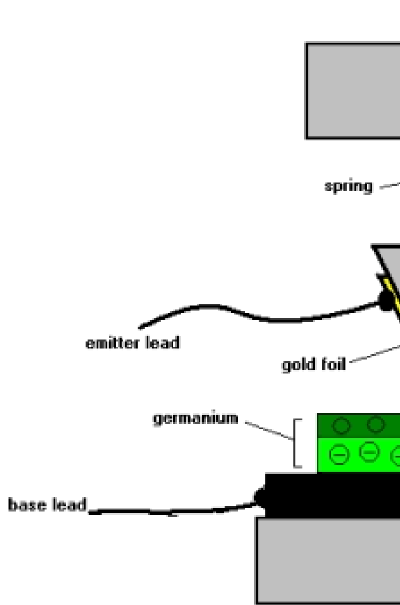
John Bardeen, William Shockley, and Walter Brattain (Bell Laboratories) [1]. 1947.

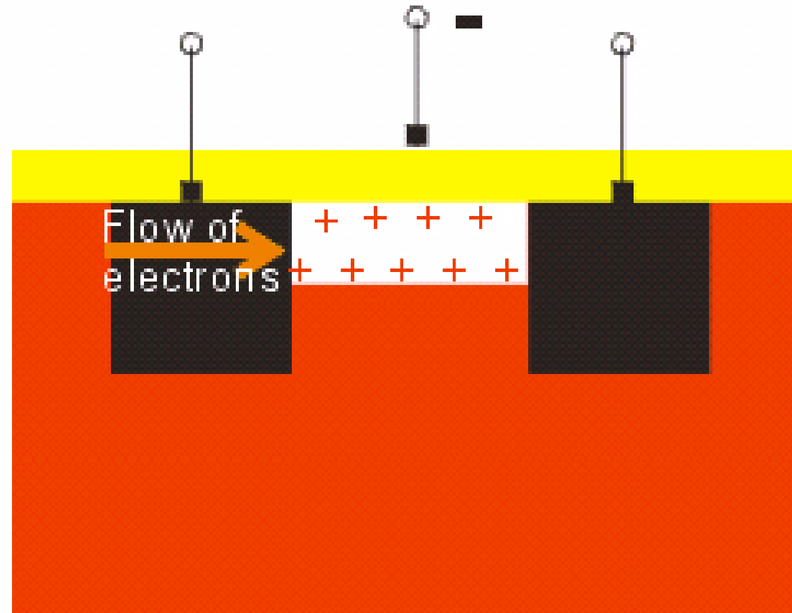


A PCB with discrete elements [12].

INTRODUCTION

FIRST TRANSISTOR

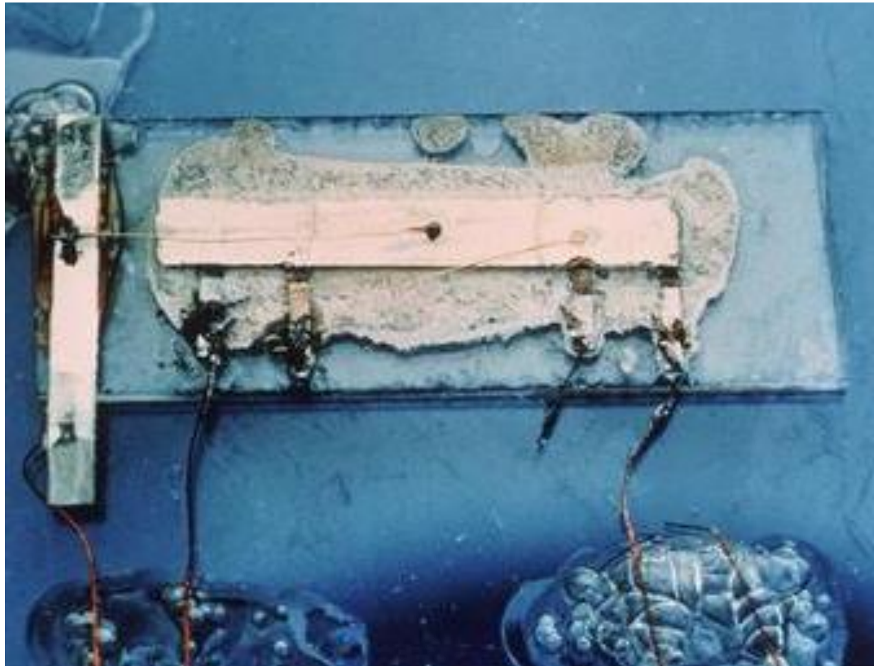




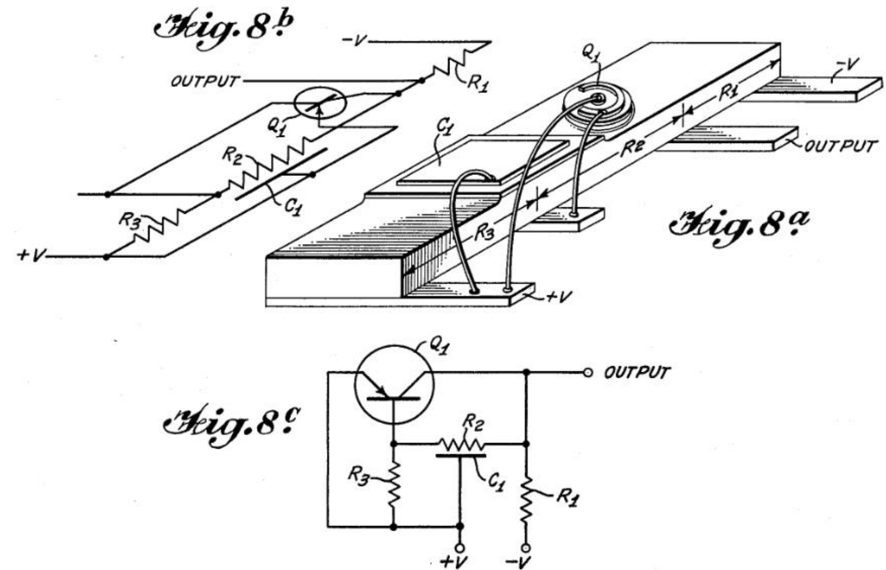
John Bardeen, W nents [12].
Walter Brattain (Bell Laboratories) [1].
1947.

INTRODUCTION

FIRST INTEGRATED CIRCUIT



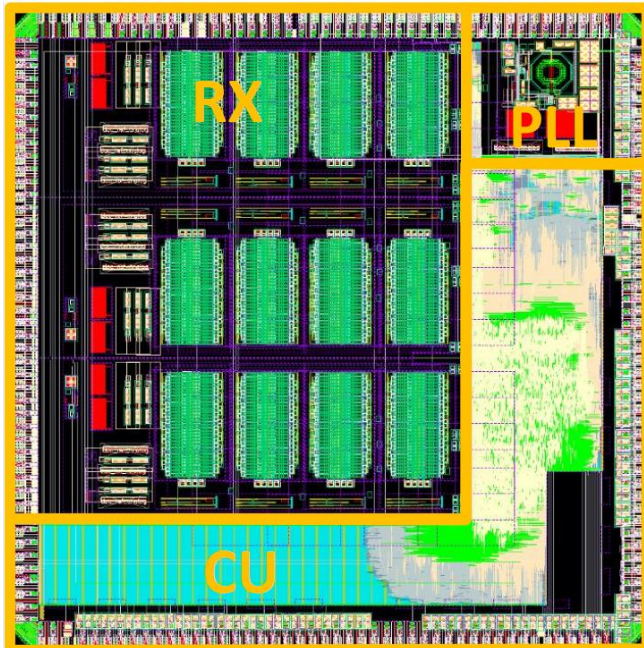
Jack Kilby's integrated circuit [3]. A single transistor IC.



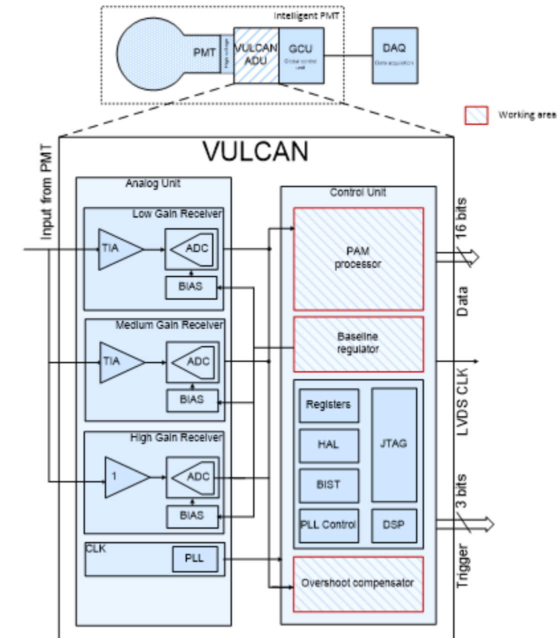
First patented integrated circuit [4]. 1959.

INTRODUCTION

MODERN INTEGRATED CIRCUITS



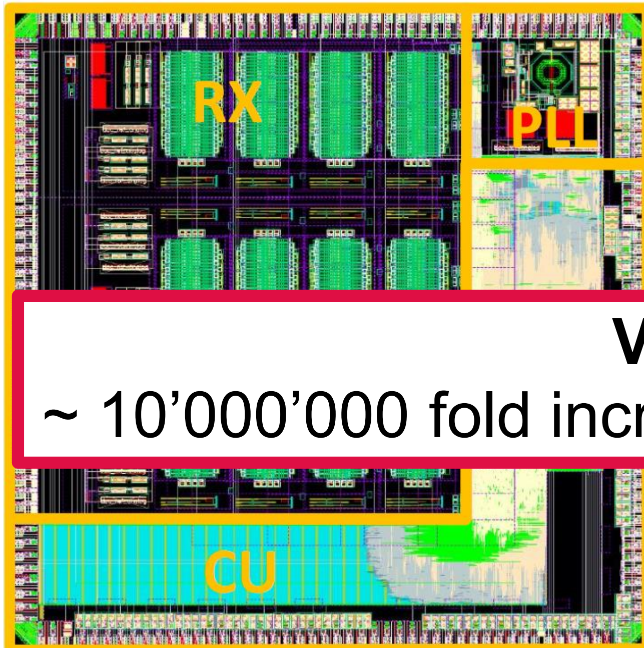
The VULCAN IC for PMT readout.
Size: 4.5 × 4.5 mm.
Technology: 65nm CMOS TSMC [7].

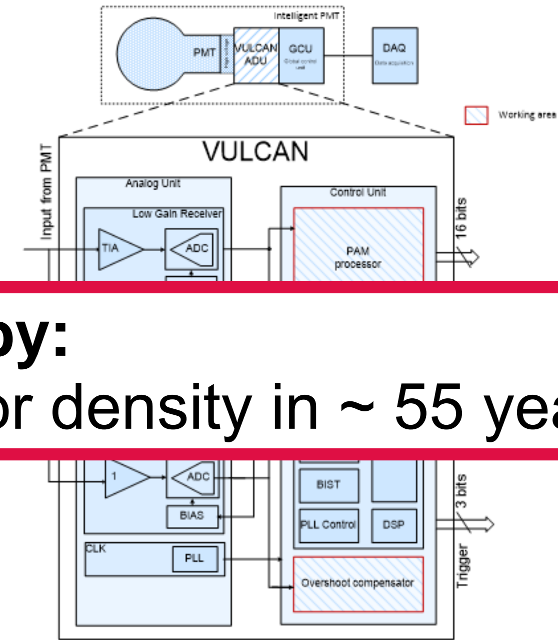


A diagram of the VULCAN chip.
Forschungszentrum Jülich GmbH – ZEA-2

INTRODUCTION

MODERN INTEGRATED CIRCUITS





VULCAN vs. Kilby:

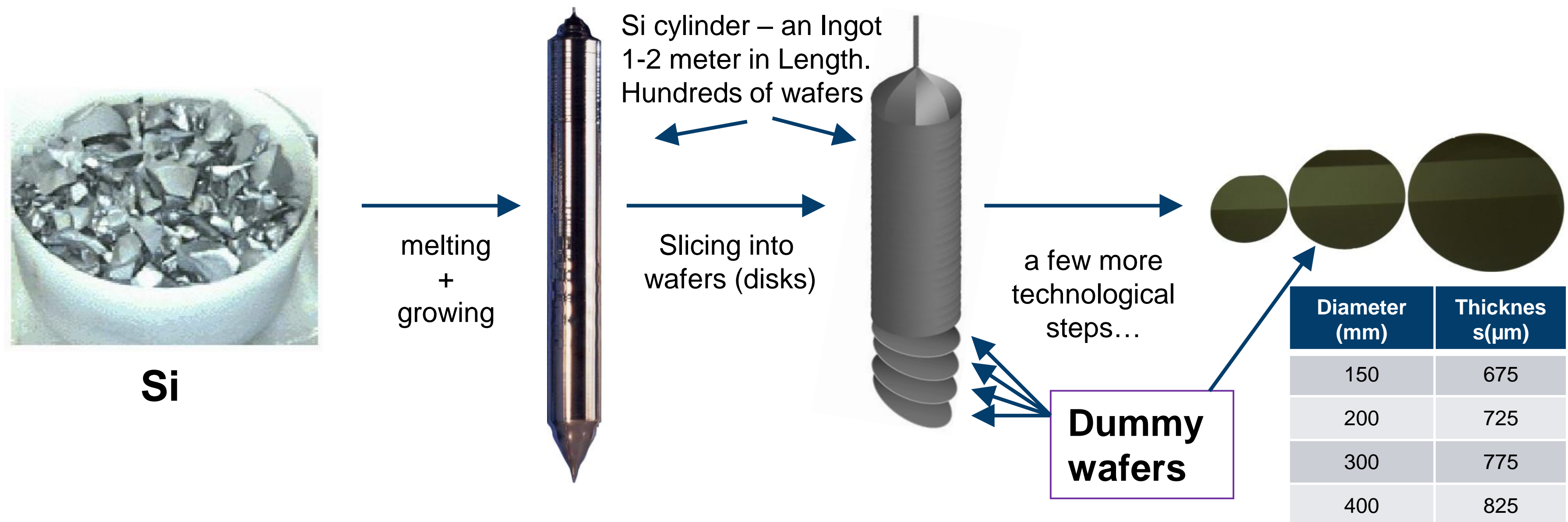
~ 10’000’000 fold increase in transistor density in ~ 55 years

The VULCAN IC for PMT readout.
Size: 4.5 × 4.5 mm.
Technology: 65nm CMOS TSMC [7].

A diagram of the VULCAN chip.
Forschungszentrum Jülich GmbH – ZEA-2

TRENDS AND ISSUES OF MODERN IC'S

CMOS TECHNOLOGY – BASIC STEPS I



Diameter (mm)	Thickness(µm)
150	675
200	725
300	775
400	825

TRENDS AND ISSUES OF MODERN IC'S

CMOS TECHNOL

BLADE

INK

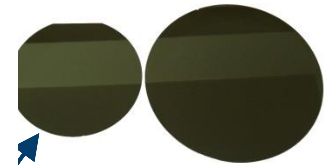
SCREEN

TEMPLATE

PAPER

BASE

Si



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150	675
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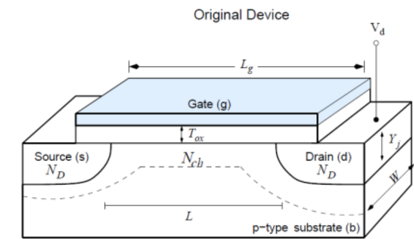
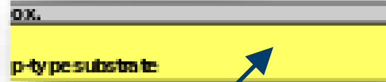
CMOS TECHNOLOGY – BASIC STEPS II

To describe transistor formation on a wafer a single slide is not enough. Only a few major steps are shown below:



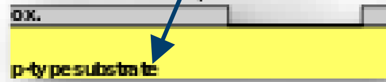
Cross-sectional diagram of a transistor

1. Grow field oxide



WAFER

2. Etch oxide for pMOSFET



3. Diffuse n-well

4. Etch oxide for nMOSFET

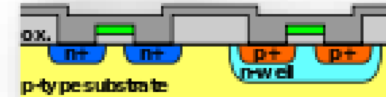
5. Grow gate oxide

6. Deposit polysilicon

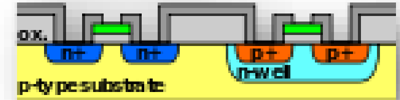
7. Etch polysilicon and oxide

8. Implant sources and drains

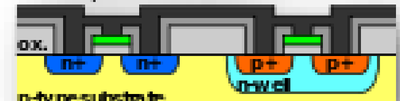
9. Grow nitride



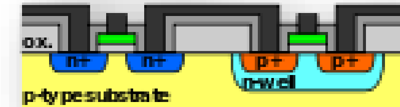
10. Etch nitride



11. Deposit metal



12. Etch metal



Figures from [11]

TRENDS AND ISSUES OF MODERN IC'S

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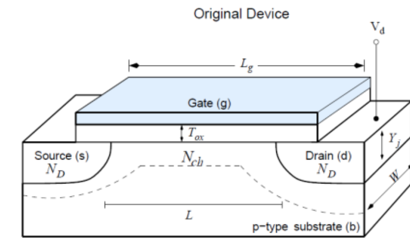
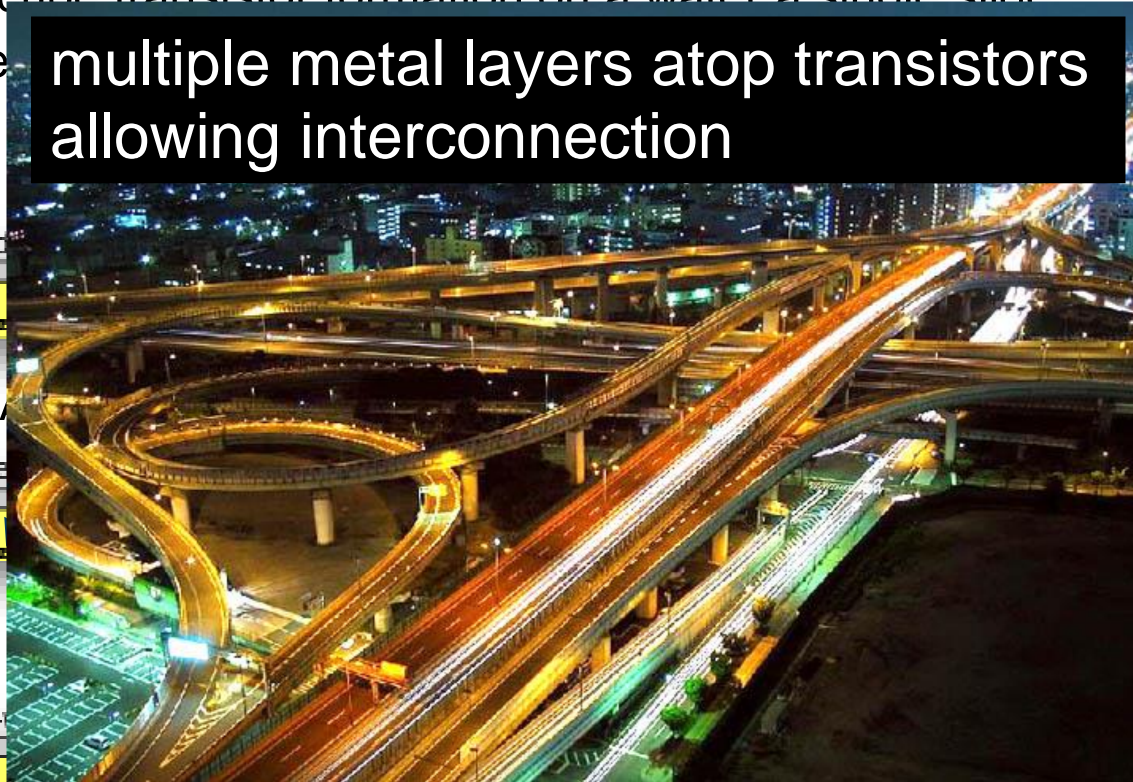


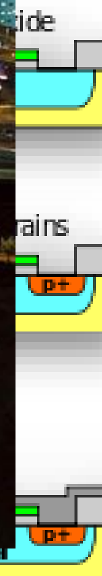
Cross-sectional diagram of a transistor

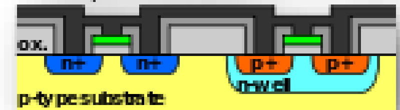


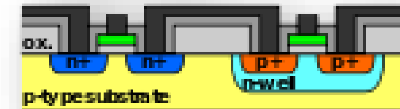
1. Grow field

2. Etch oxide

3. Diffuse n-







Figures from [11]

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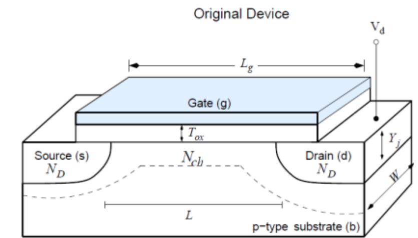


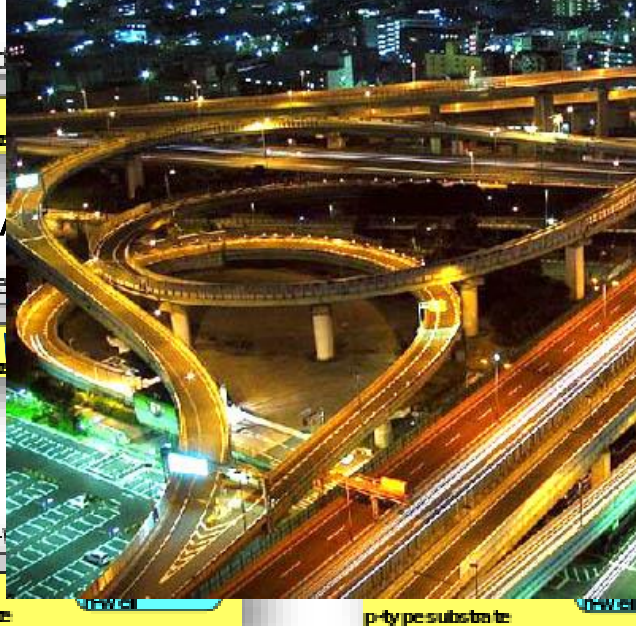
To describe transistor formation on a wafer a single slide is not e…

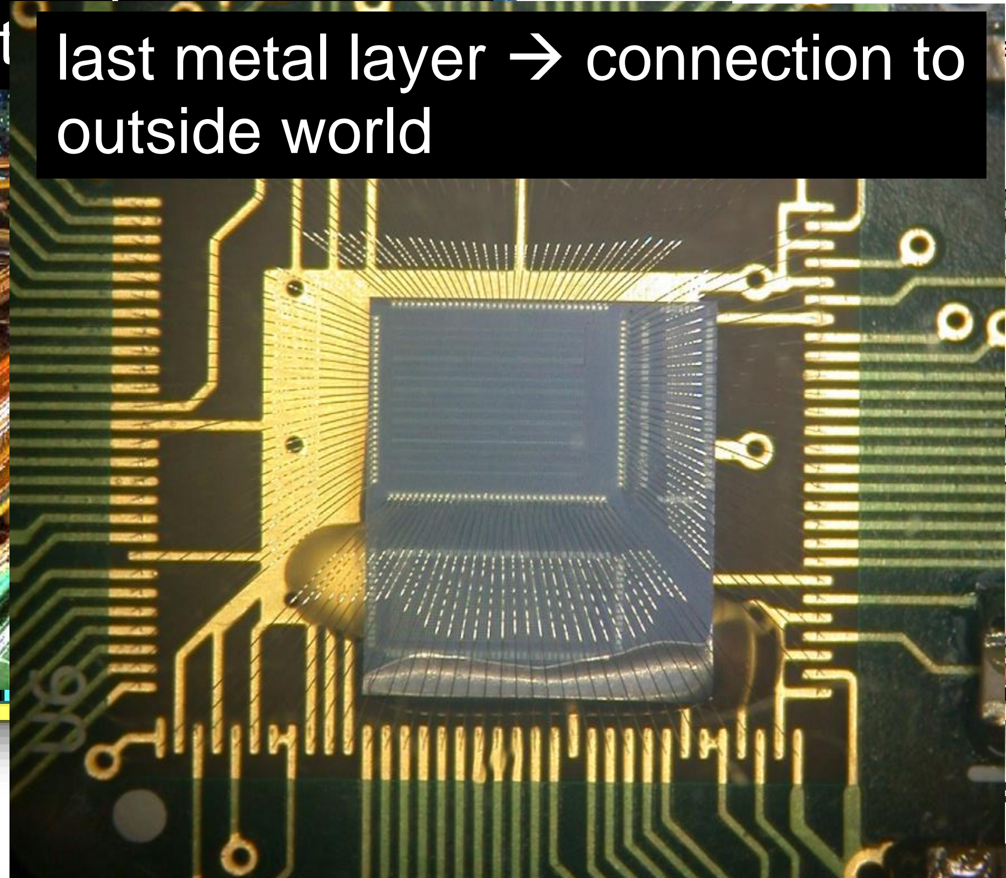
…agram

1. Grow field…
ox.
p-type substrate

2. Etch oxide…
ox.
p-type substrate

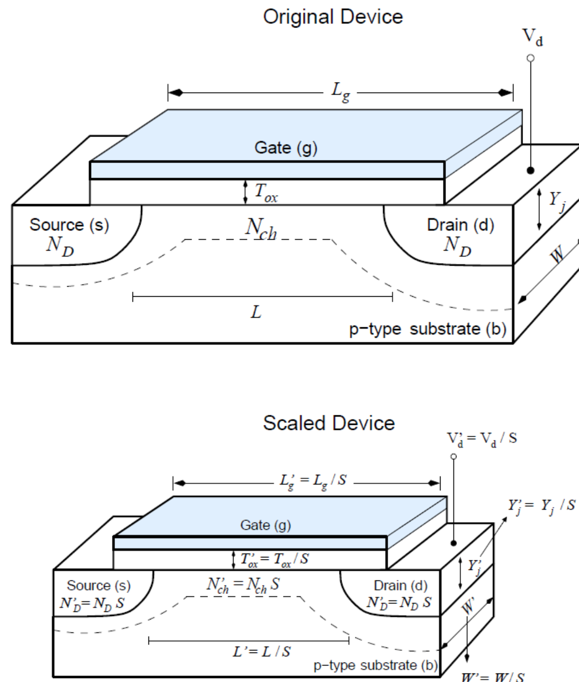
3. Diffuse n-…
ox.
p-type substrate
p-type substrate
p+

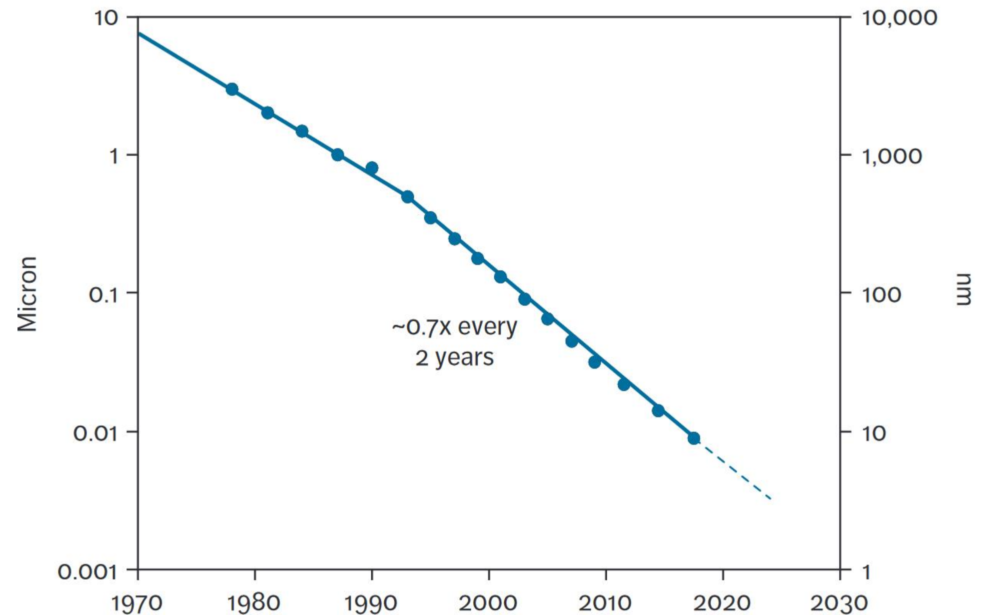




TRENDS AND ISSUES OF MODERN IC'S

TRENDS: TRANSISTOR SCALING



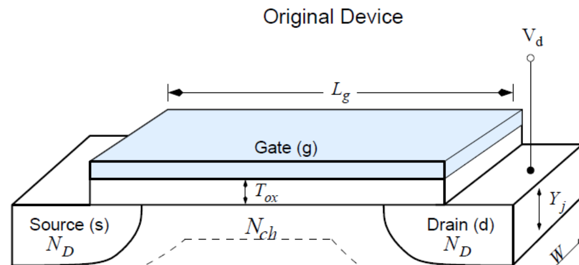


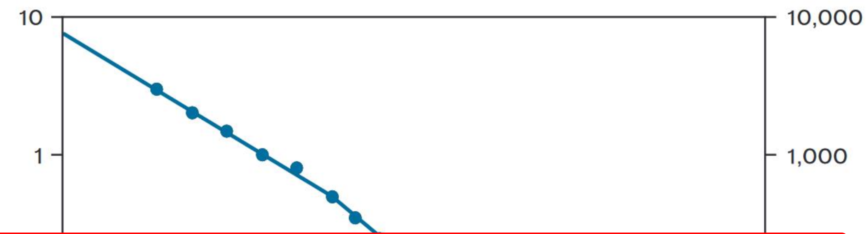
Transistor scaling → downscaling [6].

CMOS Technology node vs. year.
"Moore's low in action" [5].

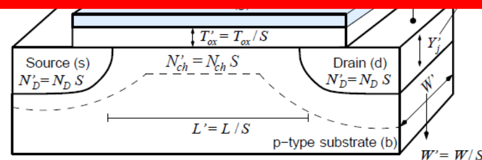
TRENDS AND ISSUES OF MODERN IC'S

TRENDS: TRANSISTOR SCALING





Today - "A technology node is simply a commercial name for a generation of a certain size and its technology, and does not represent any geometry of the transistor."



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CMOS Technology node vs. year.
"Moore's low in action" [5].

TRENDS AND ISSUES OF MODERN IC'S

SCALING: PROs

- Functionality per unit area increases
- Power per function decreases
- Transistor delay decreases
- Cost per single IC decreases
- Radiation hardness increases (thinner gate oxide)
- …

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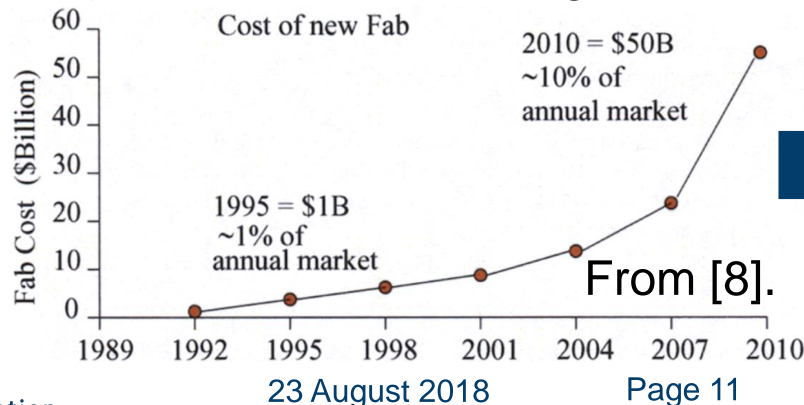
SCALING: CONNs (NOT A FULL LIST)

- Power density increases (more transistors per area, heat dissipation critical)
- Leakage current increases (static power consumption)
  - cure: high-k materials
- Probability of tunneling increases (unstable transistor operation)
  - cure: triplicated logic / majority voting → at the cost of chip area
- Metal interconnection delay increases (RC-delays)
  - collides with transistor speed increase
  - interconnections consume more area than transistors
  - cure: low-k materials
- Analog / RF designs benefit less (lover voltage, shorter channel → bad signal control)
  - mixed signal / analog IC design more complex, analog signal degradation
- Soft errors increase (radiation causes wrong data in memory cells)



From [8].

2018: only five foundries with ≤ 28nm CMOS

Scientific Challenges
SCIENCE
Electronic ZEA-2 Systems
Applications and Methods

TRENDS AND ISSUES OF MODERN IC'S

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SCALING: CONs (NOT A FULL LIST)

- Power density increases (more transistors per area, heat dissipation critical)
- Leakage current increases (static power consumption)
  - cure: high-k materials
- P
- M
  - collides with transistor speed increase
  - interconnections consume more area than transistors
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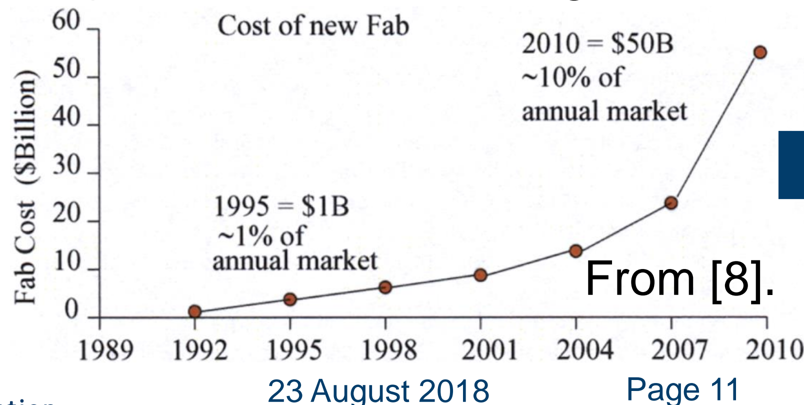
FINALLY: there are > 600 articles on the researchgate stating that the scaling will soon end …



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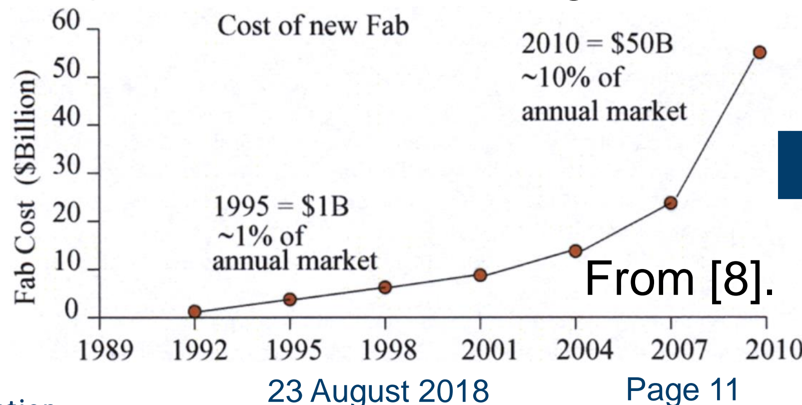
FINALLY: there are > 600 articles on the researchgate stating that the scaling will soon end …

..although, some were predicting the end @ ~ 100nm, …and we are already @ 7nm…



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TRENDS AND ISSUES OF MODERN IC'S

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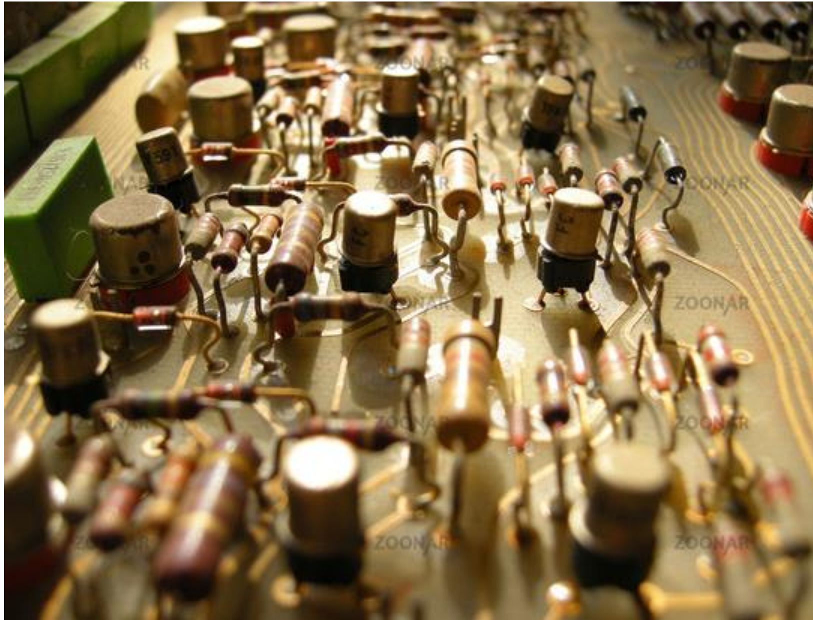
CONs – SYSTEM LEVEL



PCB from 60's [12].

Modern PCB: same concept from 60s :

- Bulky
- Trace number limited, traces long - RC-delays
- Multiple ICs → "memory and bandwidth walls"

3D INTEGRATION TECHNOLOGY

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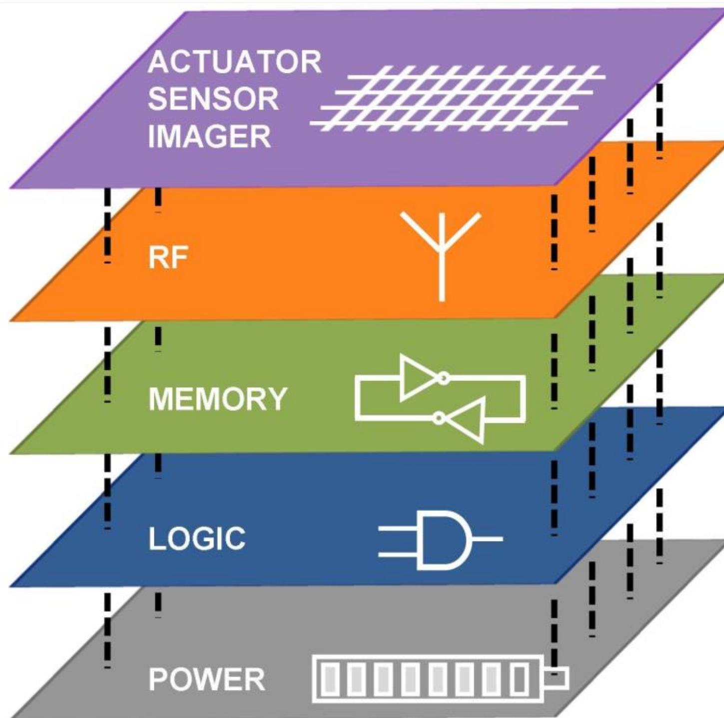
THE CONCEPT – USING 3rd DIMMENSION



A diagram of a 3D chip with mixed technologies [10].

PROs

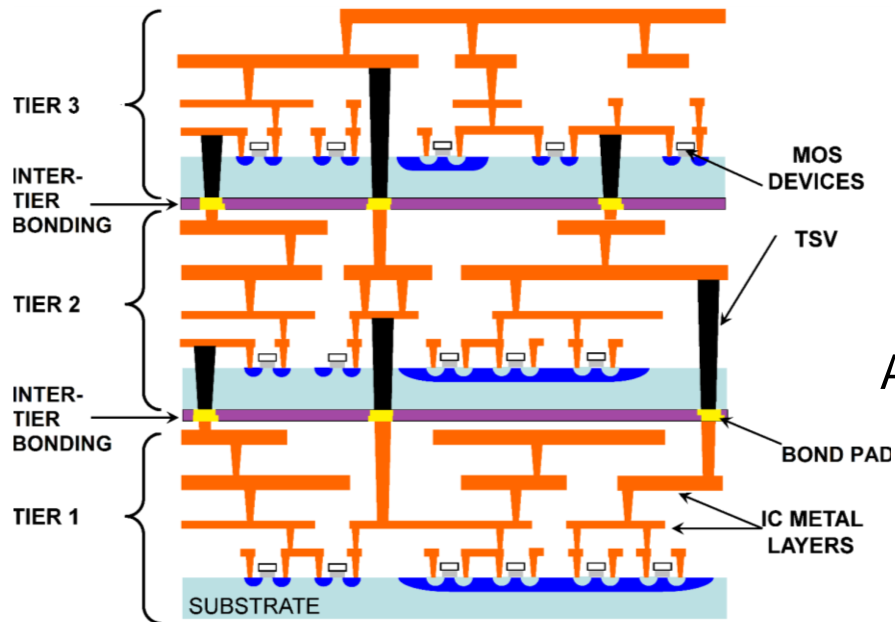
- Mix technologies → best “nm” for functionality
- Less PCB →ICs stacked, PCB RC-delays low
- Less than mm interconnections – IC RC-delays low
- Large buses → high bandwidth
- Very large memory elements
- Also MEMS and CMOS mixing

CONs

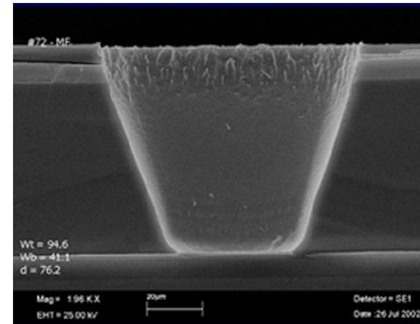
- Not mature - high price, high production risks
- No single development tool (EDA)
- High transistor density per volume area – heat dissipation high
- low yield

3D INTEGRATION TECHNOLOGY

TECHNOLOGY ENABLERS

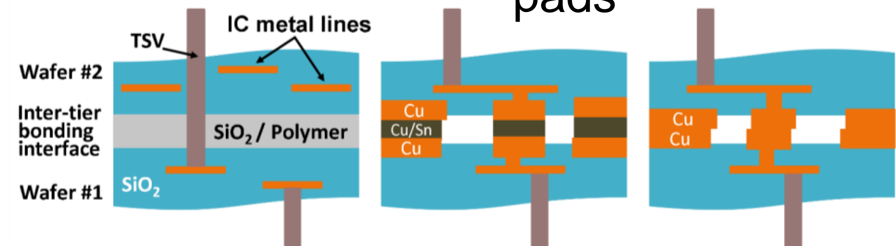


Cross-sectional diagram of a 3D-chip [10].



A through silicon Via [11]

Wafer to Wafer bonds pads

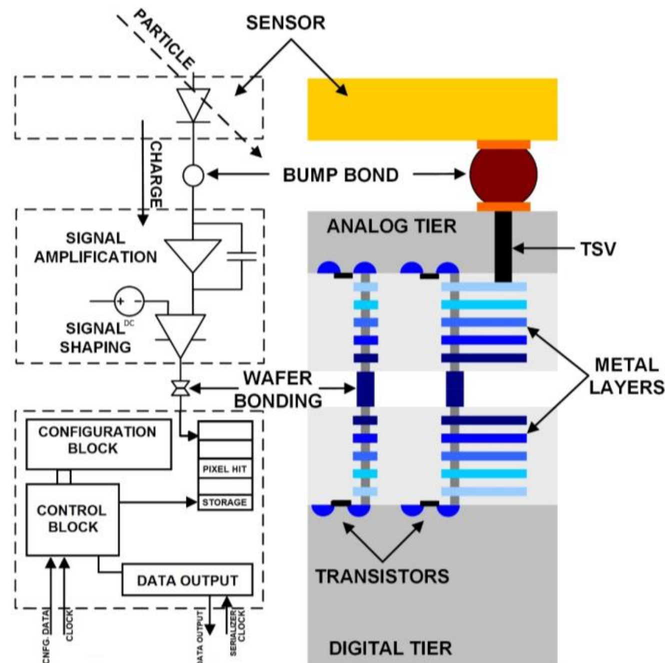


Technology enablers [11]:

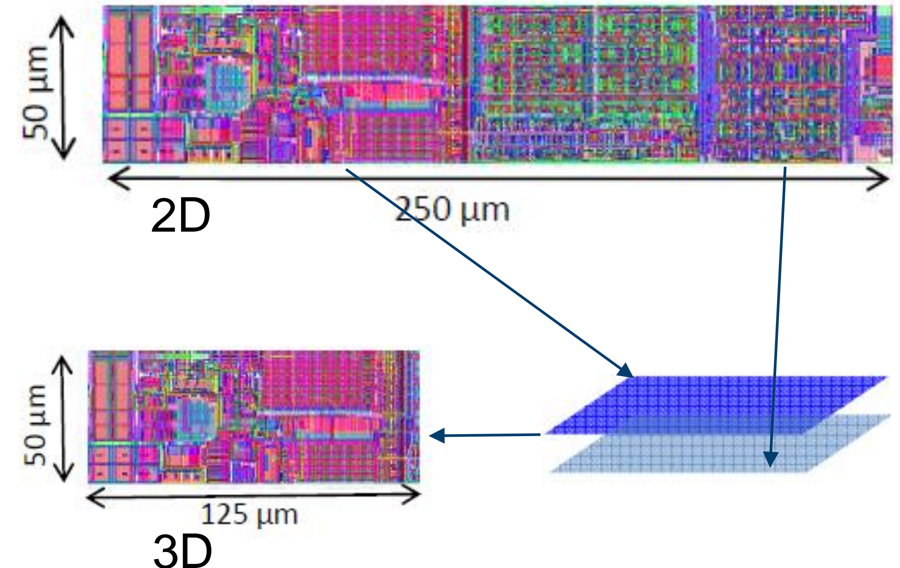
- TSV (electrical / mechanical connection)
- Wafer-to-Wafer bonding (same as above)
- Wafer thinning

CURRENT STATE OF 3D INTEGRATION

EXAMPLE I: READOUT IC PROTOTYPE FOR ATLAS PIXEL DETECTOR



Smaller detector pixel size, separation of analog and digital circuits [10].

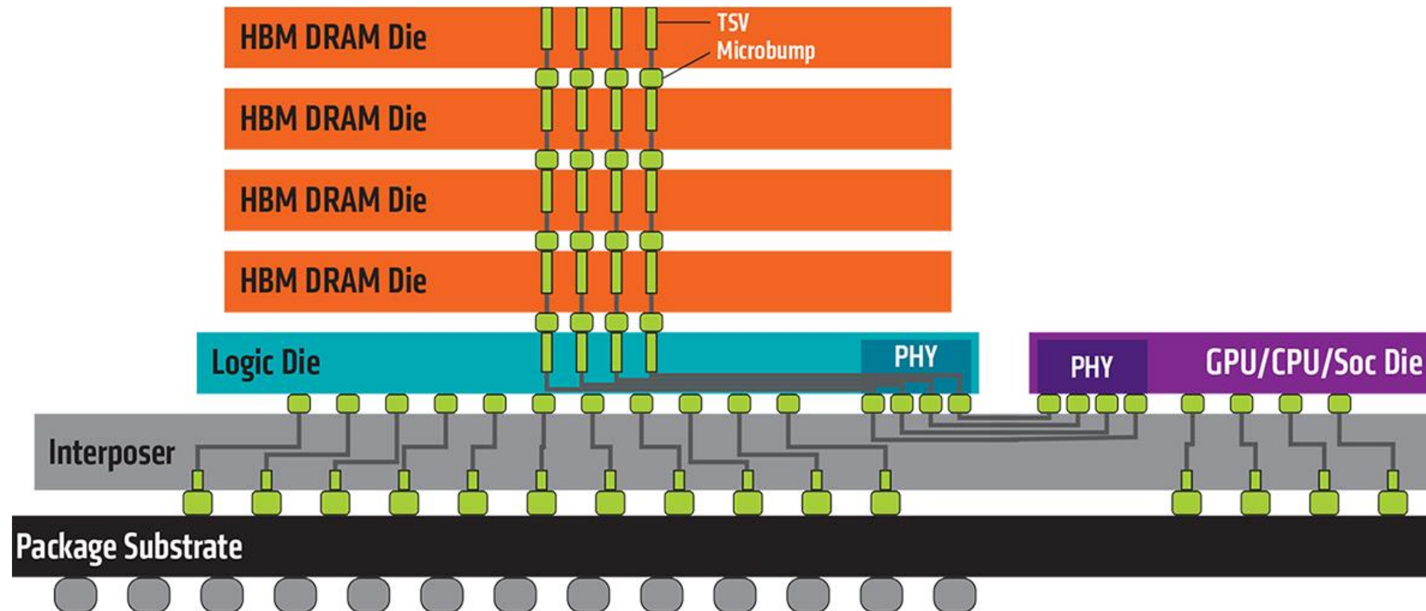


Comparison of layouts of 2D and 3D ATLAS pixel readout prototypes:

- Comparable amount of transistors
- Footprint twice as small.

CURRENT STATE OF 3D INTEGRATION

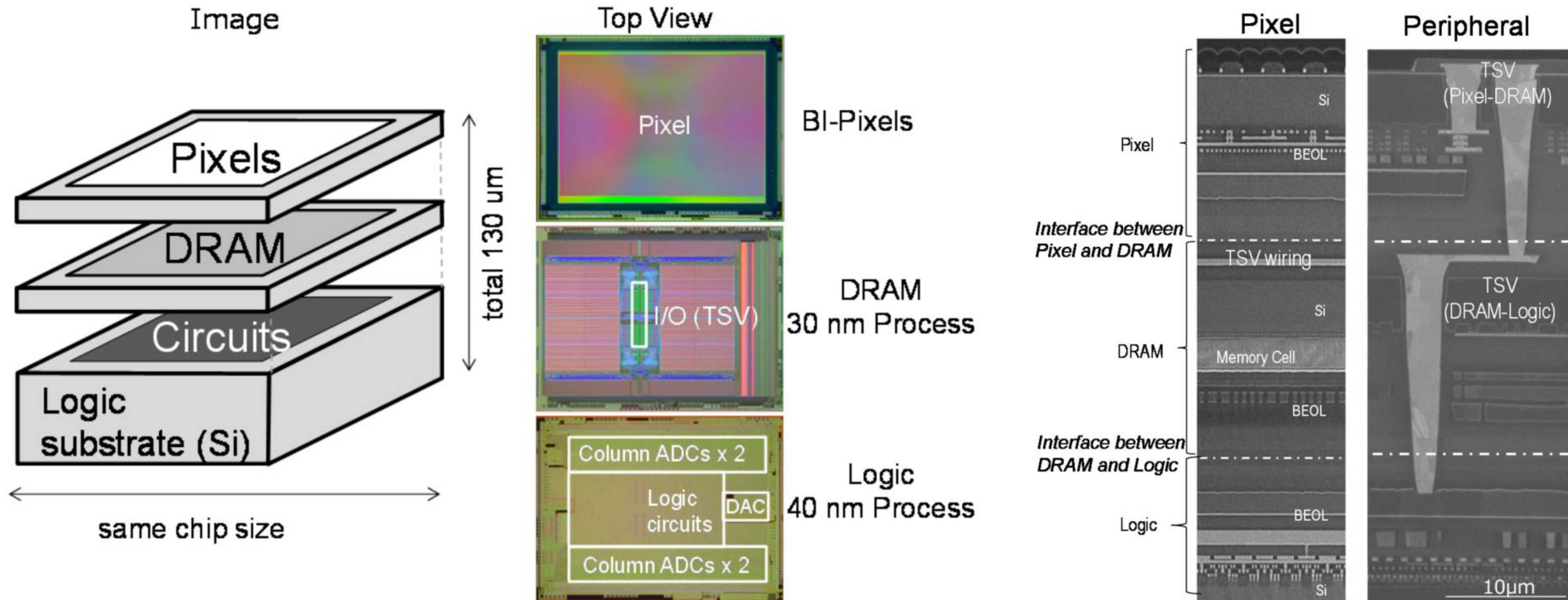
EXAMPLE II: NVIDIA



Reason: smaller form factor, larger memory – GPU bus / interface, higher data speed. Example of 3D and 2.5D mixing (interposer) – avoiding PCB resources [www.nvidia.com].

CURRENT STATE OF 3D INTEGRATION

EXAMPLE III: SONY IMAGE SENSOR



Reason: technology mixing, speed increase – super slow motion video rate of ~ 1000fps [www.sony.com].

CURRENT STATE OF 3D INTEGRATION

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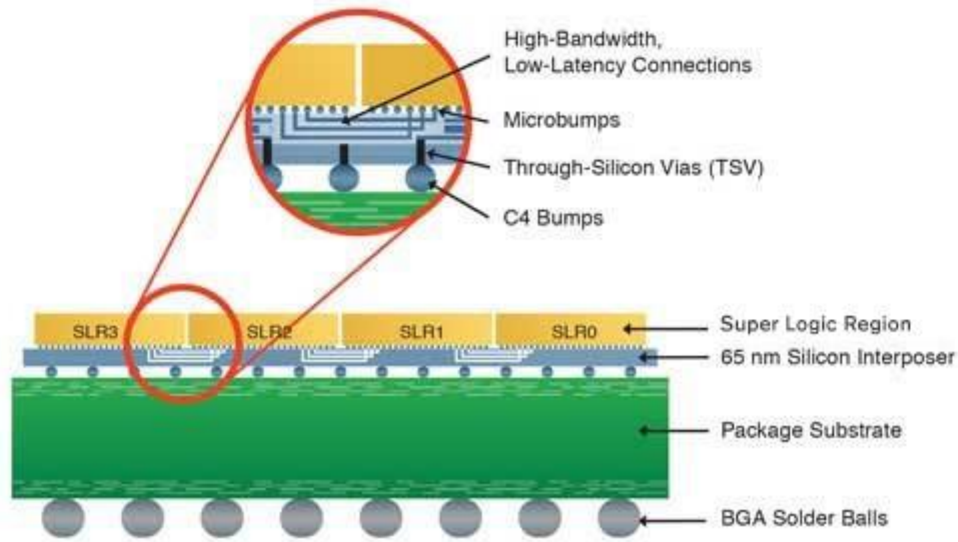
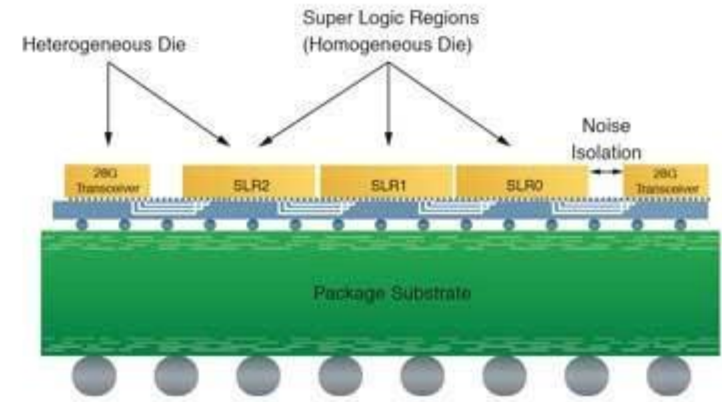
EXAMPLE III: XILINX FPGA



FPGA Enabled by SSI Technology



Heterogeneous 3D FPGA with Integrated 28G Transceivers

Reason: technology mixing. High speed data rates. Example of 2.5D integration [www.xilinx.com].

SUMMARY

- Semiconductor technology (Si based) is a very robust, universal, mature tool, used for majority of ICs and sensors on the market. Attempts for scaling down beyond 7nm will continue to keep pace with market demands.

- 3D integration is one of the “alternatives” offering functionality increase by mixing different technologies inside a single stacked IC. Still in its infancy to be widely accepted by market.

- WRT other “alternatives” to more-than-moore technologies, the 3D integration seems to be the easiest one as all technology enablers have been used separately for a long time already.

THANK YOU!

REFERENCES

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[1] https://www.aps.org/programs/outreach/history/historicsites/transistor.cfm

[2] James H. Collins "The genius who put the jinn in the radio bottle", *Popular Science" Vol. 1, No. 1, May 1922, p. 31*

[3] Winston, Brian (1998). Media Technology and Society: A History : From the Telegraph to the Internet. Routledge. p. 221. ISBN 978-0-415-14230-4.

[4] U.S. Patent 3,138,743 J.S. Kilby

[5] M. T. Bohr and I. A. Young, "CMOS Scaling Trends and Beyond," in *IEEE Micro*, vol. 37, no. 6, pp. 20-29, 2018.

[6] R. Jaramillo-Ramirez, J. Jaffari and M. Anis, "Variability-aware design of subthreshold devices," *2008 IEEE International Symposium on Circuits and Systems*, Seattle, WA, 2008, pp. 1196-1199.

[7] C. Grewing, "A new ADC chip Vulcan for PMT readout", International Workshop on Next Generation Nucleon Decay and Neutrino Detectors (NNN16), 2016

[8] N. Z. Haron and S. Hamdioui, "Why is CMOS scaling coming to an END?," *2008 3rd International Design and Test Workshop*, Monastir, 2008, pp. 98-103.

[9] V. Chandra and R. Aitken, "Impact of Technology and Voltage Scaling on the Soft Error Susceptibility in Nanoscale CMOS," *2008 IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems*, Boston, MA, 2008, pp. 114-122.

[10] D. Durini, "High Performance Silicon Imaging. Fundamentals and Applications of CMOS and CCD sensors", 2014

[11] Garou, Philip & Bower, Christopher & Ramm, Peter. (2011). Handbook of 3D Integration, Volume 1 and 2.

[12] www.wikipedia.com